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Silicon Nanowire Biosensors for Healthcare and Environmental Control

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Notes

The following publications are made so far from this research work:

1. Hakim MMA, Tanzeem, Sun K and Ashburn P "Low Cost Mass Manufacturable Silicon Nano-Sensors for Detection of Molecules in Gas Phase," SF Journal of Nanochemistry & Nanotechnology, vol. 1, pp. 1006: 1-11, 2018.

2. Tanvir Alam Shifat, Rubiya Nila, Muktadir Imam Jan and M. M. A. Hakim, "Bias dependent non-linear electrical characteristics of poly-silicon nanowire and assessment of biosensing application using liquid gate," in 9th International Conference on Electrical and Computer Engineering 20-22 December, Dhaka, Bangladesh, 2016.

3. Laila Parvin Poly, Md. Asrarul Haque and M. M. A. Hakim, "An investigation of the effects of doping and thickness on the electrical characteristics of polycrystalline silicon nanowire biosensors," in 9th International Conference on Electrical and Computer Engineering 20-22 December, Dhaka, Bangladesh, 2016.

4. A. B. Siddique, K. A. Rahman, M. N. Alam, K. Hasan and M. M. A. Hakim, "Physical understanding on the interface states and grain boundary defects of polysilicon nanowires," submitted for publication in the 10th International Conference on Electrical and Computer Engineering to be held on 20-22 December, Dhaka, Bangladesh, 2018.

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T_L	Temperature
$E_{\square}$	Perpendicular electric field
E//	Parallel electric field
μ_{AC}	Mobility limited by scattering with acoustic phonons
μ_{sr}	Mobility limited by surface roughness
μ_b	Mobility limited by scattering with optical intervalley phonons
τ_n	Electron lifetime
τ_p	Hole lifetime
E_g,	Bandgap
N	Doping concentration
L	Grain size

ϵ	Dielectric permittivity
V_B	Barrier height
J	Current density
σ	Conductivity
μ_n	Electron mobiliyy
μ_p	Hole mobility
R_{TD}	Recombination rates through the donor-like trap
R_{TA}	Recombination rates through acceptor-like trap
Q_T	Trapped charge
$g_D(E)$	Density of donor-like trap states
$g_A(E)$	Density of acceptor-like trap states.
f_A	Occupation probability for acceptor-like traps
f_D	Occupation probability for donor-like traps
SRH	Shockley-Read-Hall
DOS	Density of states
W	Channel Width
t_{ox}	Oxide Thickness
t_{si}	Polysilicon Thickness
$t_{nitride}$	Nitride Thickness
$t_{silicon}$	Silicon Thickness (n-type)
$t_{backgate}$	Back Gate Thickness
p^+	Source and Drain Dopant Density
p^+	Polysilicon Doping Density
n^+	Silicon Substrate Doping Density
σ_{ae}	Capture Cross Section of Electrons in Acceptor –like States
σ_{ah}	Capture Cross Section of Holes in Acceptor –like States
σ_{de}	Capture Cross Section of Electrons in Donor –like States

σ_{dh}	Capture Cross Section of Holes in Donor –like States
N_{TA}	Density of Acceptor-like Tail States
N_{TD}	Density of Donor-like Tail States
N_{GA}	Density of Acceptor-like Gaussian States
N_{GD}	Density of Donor-like Gaussian States
W_{TA}	Decay Energy for Acceptor-like Tail States
W_{TD}	Decay Energy for Donor-like Tail States
W_{GA}	Decay Energy for Acceptor-like Gaussian States
W_{GD}	Decay Energy for Donor-like Gaussian States
E_{GA}	Energy of Gaussian for Acceptor-like States
E_{GD}	Energy of Gaussian for Acceptor-like States
σ_n	Capture Cross Section of the Trap for Electrons at Interface
σ_p	Capture Cross Section of the Trap for Holes at Interface
D_{it}	Density of Donor-like Interface Trap States

ABSTRACT

In recent years, nanowire (NW) based ultrasensitive sensors have been widely investigated for the potential of real time, high sensitivity and label-free detection. Among different nanowire materials, silicon has the potential advantage of compatibility with very large scale integration (VLSI) and complementary metal oxide semiconductor (CMOS) technologies. These benefits are some of the main reasons for the significant interest in silicon nanowire based sensors with quite a large number of studies on the detection of analytes in aqueous environment, mainly within the context of biosensing (e.g., to detect biological species like DNA, proteins and viruses etc.). However, commercial silicon NW based sensors are still unavailable for analyte detection even in aqueous environment due to the difficulty in device manufacturing processes, reproducible sensing/integration issues and most importantly, due to the unavailability of economically viable route for mass fabrication. Silicon nanowire fabrication platform comprises bottom up, top down and spacer etch processes where conventional top down/bottom up processes usually realize sensors using single crystal silicon material whereas spacer etch process realizes sensors on polysilicon material. The choice of material is application/facility dependent and each of these material platforms have own advantages/disadvantages. The performance of nanowire as biosensor is inherently dependent on the choice of materials and also on nanotechnology variables like nanowire thickness, doping etc. A rigorous study of the effects of nanowire thickness/doping on the performance of siliconnanowire based sensors are rare in the literature and there is no study available on the critical comparison of the single crystal and polycrystal silicon nanowire biosenors. We study for the first time the effect of nanowire thickness and doping concentration on the electrical characteristics of single crystal and polycrystalline silicon nanowire biosensors and compare the performance of single crystal/polycrystal silicon nanowire biosensors to achieve a performance benchmark of sensors realized in these two material platforms. The intention is to appraise in depth the choice of nanotechnology variables for chosen material platforms for appreciable sensing. For nanowire thicknesses of 100 nm and 75 nm, a plausible sub-threshold slope around 100 mV/decade for a viable biosensor operation is achievable only if doping concentration is $2\times10^{16}/cm^3$ or below both for single crystal and poly Si nanowires. For a 50nm nanowire thickness a relatively wide doping concentration range with a maximum doping up to $4\times10^{17}/cm^3$ is viable for biosensor design while maintaining decent sub-threshold characteristics. The widest range of doping concentrations can be chosen for 25nm and 10nm nanowire thicknesses with a maximum doping up to $10^{18}/cm^3$ for feasible biosensor design using single crystal and polycrystalline silicon nanowires. In general poly Si NW shows inferior characteristics than single crystal Si NW. However, for 10nm, Si NW single crystal & poly Si NW show same sub-threshold slopes at all doping densities. Considering the fact that spacer etch process provides the cheapest & mass manufacturable platform for biosensor fabrication using poly Si material in comparison to the available single crystal platforms, it can be decided that poly Si NW biosensor with Si thickness $\leq$ 10nm is the possible commercial route of sensor fabrication with similar performance like single crystal silicon nanowires.

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CHAPTER 1

1. INTRODUCTION

A nanowire is an extremely small structure, typically with diameters on the order of few nanometers up to 100nm. Silicon nanowire is one of the 1D nano-structures that has emerged as the promising sensing nanomaterial upon its unique mechanical, electrical and optical properties [1]. Due to its small size and large surface-to-volume ratio, the depletion and accumulation of charge-carriers produced by specific binding of biological macromolecule on the surface affects the entire cross sectional conduction pathway, that's why NW devices give extraordinary sensitivity when compared to other transducers reported in the literature [2]. Si-NW chemical sensors operated as field-effect transistors (FET) are currently the most commonly used structure [2]. The application of silicon nanowire as a sensing nanomaterial for detection of biological/chemical species and gases has gained attention due to its unique properties [2-6]. Though this advantage of nanowires has been used to sense ions, proteins, DNA and viruses, some important issues yet remain to be resolved before its mass commercialization. Material selection and associated cost, appropriate choice of thickness, length, doping of nanowires and reproducible sensing are the outstanding issues that have to be specified.

In general, the silicon nanowire nanofabrication toolbox consists of two techniques such as bottom-up approach and top-down approach. Generally, single crystal silicon nanowire is fabricated by using bottom-up technique. Bottom-up approach is a growth or synthesized technique of the SiNWs from bulk silicon wafers either metal catalyzed-assisted or metal catalyzed-free [1, 7]. Bottom-up nano-fabrication is in principle simple and provides many high quality materials. In recent years, many researchers have successfully fabricated SiNWs using this approach in producing a large quantity of SiNWs [7]. In these techniques, suitable methods for accurate nanowire alignment are lacking, and electrical contact formation is problematic, making it difficult to construct functional device arrays [7]. An SEM image of the bottom up grown SI NW is shown in figure 1.1. The image undoubtedly shows the location and diameter uncertainity of the grown nanowires for reproducible integration.

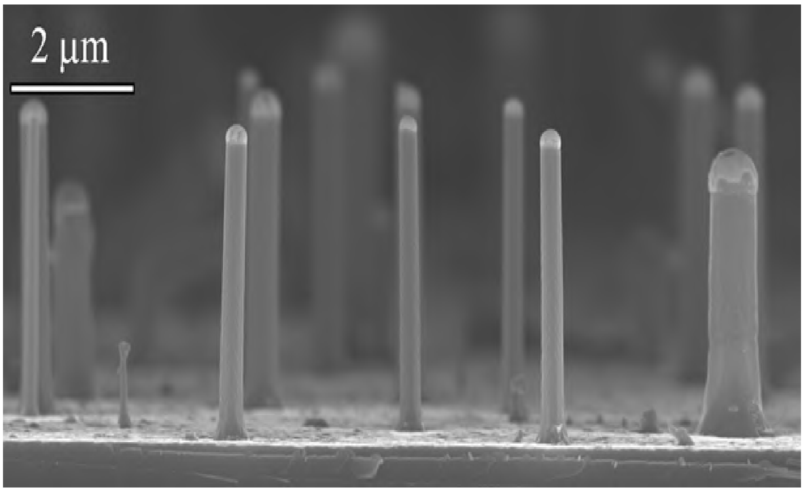

Figure 1.1: Bottom up grown nanowires (Source: Southampton nanofabrication Center)

Some expensive top-down techniques also exist for fabricating single crystal silicon nanowire thatovercome the shortcomings of bottom-up grown nanowires. Several groups used nano-patterning techniques such as deep-UV photolithography and electron beam lithography to fabricate silicon nanowires on silicon-on-insulator (SOI) substrate [8]. This has the advantage of CMOS compatibility. But the major disadvantage of this technique is the high cost associated with these advanced lithography techniques and expensive SOI wafers. Figure 1.2 shows an SEM image of top down fabricated NW processed using deep-UV photolithography.

Recently a low cost, top-down approach to nanowire fabrication has been reported that uses thin film technology and spacer etch technique [9, 10]. This approach is particularly attractive because it produces nanowires with nano-scale dimensions using mature lithography in combination with standard deposition and spacer etch techniques that are widely available in industry. More importantly, this process can be used for glass or plastic substrates suitable for the realization of low cost disposable diagnostic kits. However, in this approach, defined nanowires are usually amorphous and/ or polysilicon depending on the deposition and annealing conditions. As a result, nanowire material usually composed of grain boundaries and defects which may also affect its electrical characteristics eventually affecting biosensor performance realized in these nanowires.Figure 1.3 shows an SEM image of a polysilicon nanowire that has been processed using spacer etch.

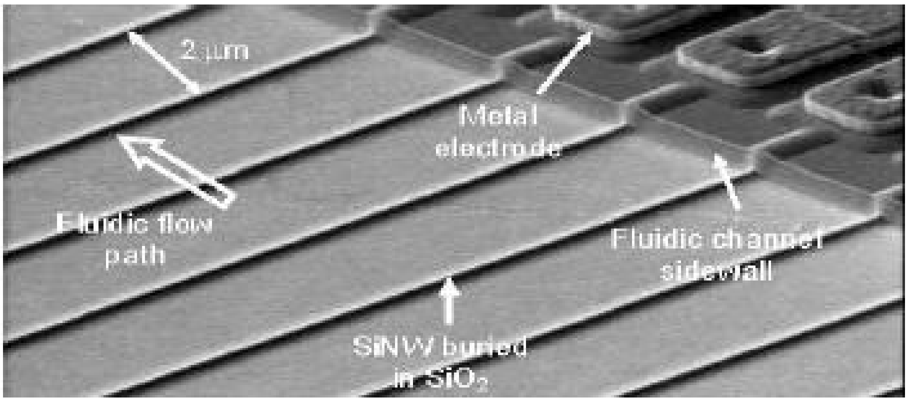

Figure 1.2: Top down nanowires processed by Deep UV lithography (Source: ref [17])

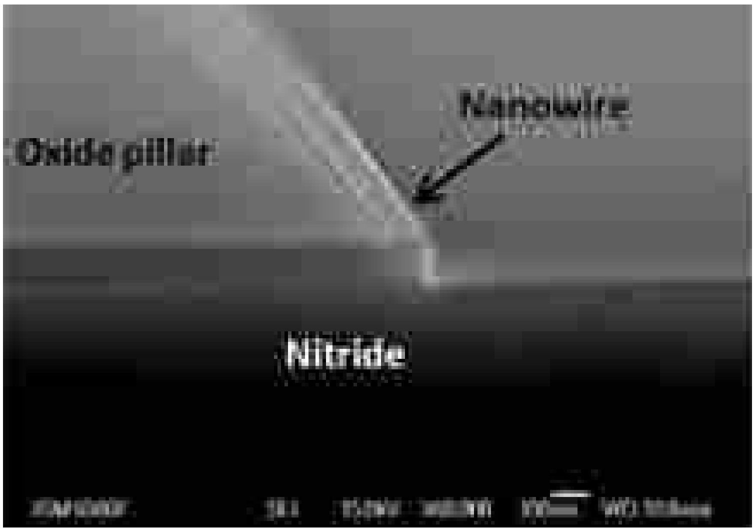

Figure 1.3: Polysilicon nanowire that has been processed using spacer etch (Source: ref [10])

The aforementioned discussion reveals that the best approach for Si NW fabrication is unclear at present time and a phenomenological development is needed for a commercial scale production. Bottom up and conventional top down approach may provide best quality silicon NWs as these approaches realize single crystal material but have difficulties in commercial grade manufacture either due to reproducible integration issues or cost. Although spacer etch has advantage of realizing NWs in a CMOS compatible process with the possibility of low cost mass manufacture, the NWs materials in this process are inherently polyslicon or amorphous. The choice of material for NW biosensor would depend on the feasible process that may enable mass manufacture in an economically viable platform in near future. However, the performance of nanowire as biosensor is inherently dependent on the choice of materials and also on nanotechnology variables like nanowire thickness, doping etc. A rigorous study of the effects of nanowire thickness/doping on the performance of silicon nanowire based sensors are rare in the literature and there is no study available on the critical comparison of the single crystal and polycrystal silicon nanowire biosenors.

In this work we report for the first time the effect of nanowire thickness and doping concentration on the electrical characteristics of single crystal and polycrystalline silicon nanowire biosensors and compare the performance of single crystal/polycrystal silicon nanowire biosensors to achieve a performance benchmark of sensors realized in these two material platforms. The intention is to appraise in depth the choice of nanotechnology variables for chosen material platforms for appreciable sensing. The effect of nanowire thickness and doping concentration on the electrical characteristics of both type silicon nanowires are investigated,which also provides the proper combination of nanowire thickness and doping concentration to ensure the sensitive operation for both type of silicon. The electrical characteristics of a p-type silicon (single crystal and poly crystal) nanowire having a nanowire length 1µm is studied at various thicknesses and doping concentrations. 10nm, 25nm, 50nm, 75nm and 100nm thick nanowires with doping density varying from $10^{16}/cm^3$ to $10^{18}/cm^3$ are investigated.

CHAPTER 2

2. BACKGROUND

This chapter summarizes the background work of accumulation mode silicon nanowire transistors, its application as biosensor and relevant theory associated with this work. Being a novel concept, this type of device attracted attention of several researchers.Works have also been reported that tried to explain the behavior of accumulation mode silicon nanowire transistors. While these works provided some focus on the transistor like behavior of simple nanowires, an extensive application could be found on biosensors which have exploited this behavior. These are discussed below:

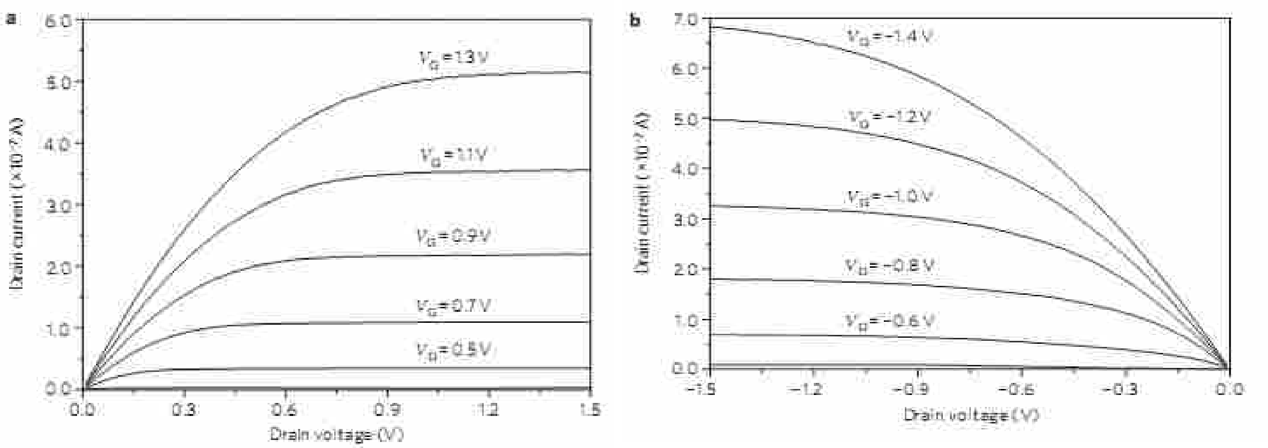

Figure 2.1: Measured output characteristics of junctionless accumulation mode silicon nanowire transistors; a) Drain current versus drain voltage for different values of gate voltages for an n-type silicon nanowire and b) drain current versus drain voltage for different values of gate voltages for an p-type silicon nanowire.The width of the nanowires, W, is 20 nm and the gate length, L, is 1 µm, such that W/L = 0.02 (courtesy: Jean-Pierre Colinge et al. [11])

2.1 Accumulation mode silicon nanowire transistor

Jean-Pierre Colingeet al.[11] first time reported that Si-NWs with a few tens of nanometers wide, thickness of 20nm and uniform doping concentrations around10^{19} cm^{-3} behave as transistor rather than simple conductor. Both p-type and n-type silicon nanowires were fabricated, and measured characteristics showed that both n-type and p-type devices exhibited transistor action. These devices showed near ideal sub-threshold slope of 64mv dec^{-1} and quite decent output characteristics. Figure 2.1and 2.2 show the measured sub-threshold and output characteristics of such accumulation mode silicon nanowire transistors.

To explain the behavior of these devices, a simulation was done [11]. Fig. 2.3 shows the operation principle of n-type accumulation mode silicon nanowire transistor. In the sub-threshold region [Fig.2.3(a)], a highly doped channel is fully depleted. At threshold voltage [Fig.2(b)], current starts to flow through the center of the channel. In the above-threshold regime [Fig.2(c)], the channel neutral n-type silicon expands in width and thickness. When the gate voltage is increased, a completely neutral channel is created [Fig.2(d)] as the gate voltage forces saturation of the drain current.

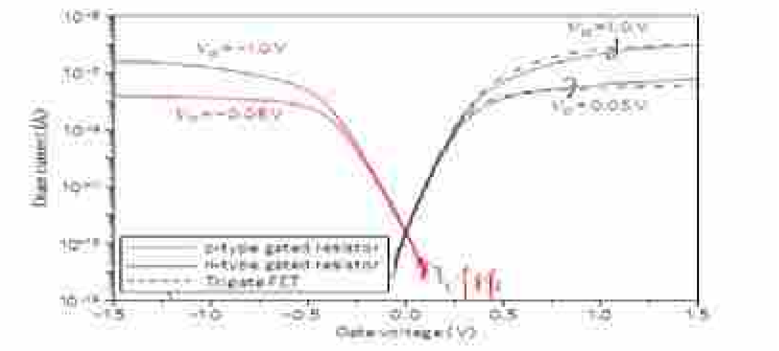

Figure 2.2: Measured sub-threshold characteristics of junctionless accumulation mode silicon nanowire transistors. Drain current versus gate voltage for drainvoltagesof50mV and1Vfor n-type and p-type silicon nanowires. The width of the nanowires are 30 nm and the gate length, L, is 1 µm(courtesy: Jean-Pierre Colinge et al. [11])

A theoretical study on the accumulation mode silicon nanowire transistor was done by Elena Gnani et al. [12] to explain near ideal subthreshold slope, large on state current and excellent DIBL. It is reported that the good subthreshold slope is due to the fixed voltage drop (Δφ) across the silicon nanowire and the oxide under complete depletion of the channel. This lets the potentialon the symmetry axis of the nanowire to linearly change with the gate voltage, with a linearity factor equal to 1. The reason for large on-state current, which is quite comparable with that of the undoped NW FET with same geometry is attributed to the absence of impurities at the conducting region and reduced surface-roughness scattering. The good DIBL is due to the reason that on-state current injection is modulated by the radius of the neutral region rather than the thermionic injection above the barrier and the electrostatic effect of the drain voltage is screened by the mobile charges within the channel.

In order to understand the behavior of the long-channel accumulation mode silicon nanowire transistor, Juan P. Duarteet. al. [13] proposed a simple analytical expressions to model the bulk current characteristics of silicon nanowire. This model is derived from the solution of the Poisson equation to find channel potential using the dependence of depletion region under applied gate voltage. A good agreement was found when the results were compared with numerical simulation results of ATLAS platform.

In further work of Juan P. Duarte et. al. [14] a full range drain current model accumulation mode silicon nanowire transistor was proposed with Pao-Sah electrostatic assumption and by extending the concept of parabolic potential approximation in the sub threshold and linear region including the dopant and mobile carrier charges. Based on the continuous charge model, the Pao-Sah integral is analytically solved to set a continuous drain current model. The proposed model is claimed to be appropriate for compact modeling because it continuously captures the phenomenon of the bulk conduction mechanism in all regions of device operation, including the subthreshold, linear and saturation regions.

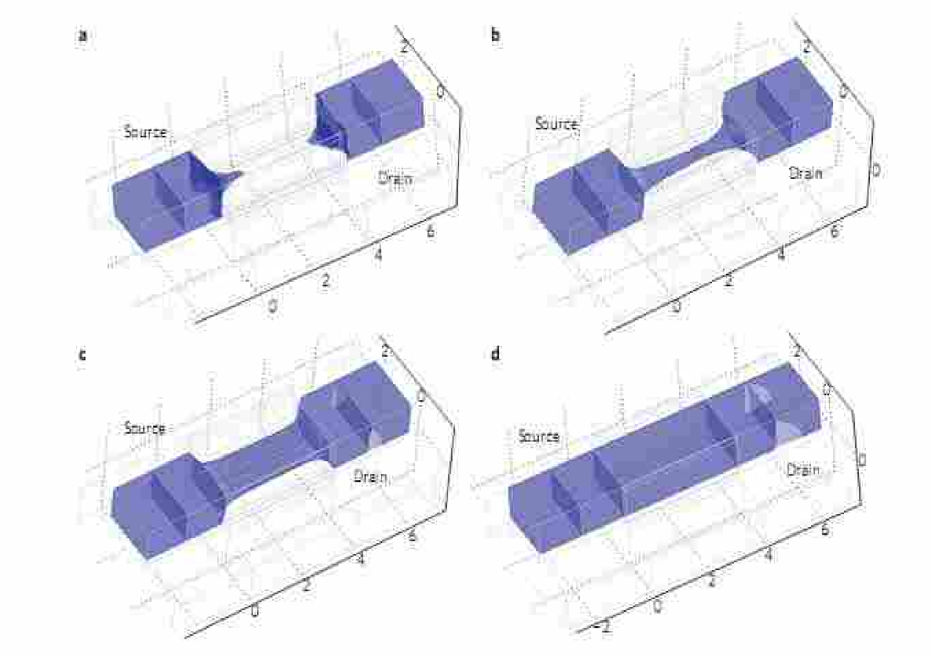

Figure 2.3: Electron concentration contour plots in an n-type accumulation mode silicon nanowire transistor. Plots are taken from simulations carried out for a drain voltage of 50 mV and for different gate voltages: below threshold (VG<VTH) the channel region is depleted of electrons (a); at threshold (VG = VTH) a string-shaped channel of neutral n-type silicon connects source and drain (b); above threshold (VG > VTH) the channel neutral n-type silicon expands in width and thickness (c); when a flat energy bands situation is reached (VG = VFB >>VTH) the channel region has become a simple resistor (d). The plots were generated by solving the Poisson equation and the drift-diffusion and continuity equations self-consistently. The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1×10^{19} cm-3(courtesy: Jean-Pierre Colinge et al. [11])

The probability of gate-all-around accumulation mode nanowire transistors using polycrystalline silicon was demonstrated by Chun-Jung Su et.al.[15] utilizing only one heavily doped poly-Si NW to serve as source, channel and drain region. In this work it was found that the fabricated gate-all-around polycrystalline nanowire transistors with a NW thickness 12 nm exhibited excellent I_{on}/I_{off} ratio of 5.2×10^6, quite a good sub- threshold slop of 199mV/dec being a polysilicon device, enhanced drive current as well as good immunity to short channel effects. It is also observed that this device exhibited lower source/drain series resistance than its inversion-mode counterpart.

2.2 Silicon NW Bio-sensor

While transistor behavior of simple silicon nanowire is interesting as a disruptive switching device, it has quite a promising application as biosensors. A typical nanowire biosensor can be a single or an array of nanowires which is laid on an insulator between source and drain [Fig. 2.4]. Electrodes of these source and drain are isolated by a protection layer. On Si-NW surface, target receptors that have the capability of immobilizing the targets, e.g. ions, DNA, proteins are attached by molecular linkers. Due to large surface to volume ratio, the charges associated with the attached molecules can deplete or accumulate entire cross sectional path way. As a result, NW conductance gets easily changed. This phenomenon resulted in the most promising breakthrough in the 21th century by possible application of simple NW devices for disease diagnosis.

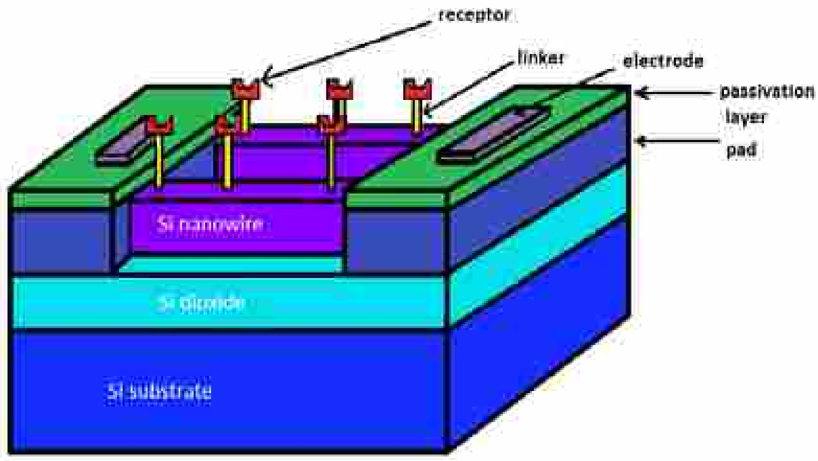

Figure 2.4: Schematic diagram of the structure of Si-NW biosensor

Table 2.1 shows a simple survey of silicon nanowire / nanoribonsthat have been used as biosensor. From this table it is evident that quite a broad range nanowire thicknesses and doping are employed for biosensor fabrication. This was mainly due to the experimental constraints of bottom up self-assembled nanowirefabrication where doping was achieved as well in a self assembled nature by gas flow adjustment. In top down method, doping was incorporated a bit arbitrarily as no information of required doping for any particular thickness was available. It is worth mentioning that low doped nanowires were expected to be highly sensitive as low gate voltages can easily deplete or accumulate nanowires. However, low doped nanowires also become highly sensitive to environmental change, which is difficult for viable biosensingapplication, as biomolecules associated signals get easily mixed up with signals generated from environmental change like moisture, presence of gaseous molecules etc.

Table 2.1: Survey of Si nanowire/nanoribbon biosensors

Year	Nanowires	Lithography[a]	Doping/Dose/ resistivity/ sheet resistance	NW Thickness	Detection limit	Ref.
2006	SOI[b], n-&p-type, pass[c] :Si_3N_4	e-beam[d] -	~10^{19}cm^{-3}	20nm	1 nM 10 pM	[16]
2007	SOI, n-&p-type	DUV[e]	10^{13} to10^{15} cm^{-2}	40nm	10 pM	[17]
2008	SOI,p-type	e-beam	14–22 Ω cm	100nm	1 nM	[18]
2008	SOI,p-type	e-beam	10^{18}cm^{-3}	100nm	1 µM	[19]
2009	SOI,n-type	DUV	5*10^{13} cm^{-2}	~80nm	1 fg/mL	[20]
2009	Poly-Si, n-type	e-beam	40–50 Ω/ cm^2	80nm	10 nM	[21]
2010	Poly-Si, n-type	e-beam	40–50 Ω/ cm^2	80nm	30 nM	[22]
2012	Poly-Si, p-type	Spacer etch	~10^{16} cm^{-3}	100nm	10 fM	[10]

a: lithography only refers to the lithography techniques for nanowires patterning, whilst optical photolithography might be used throughout other processes.
b: SOI- silicon on insulator
c: passivation layer to isolate device from analyte
d: e-beam-electron-beam lithography
e: DUV – deep-ultraviolet lithography

CHAPTER 3

3. METHODOLOGY

3.1. Device features and simulation models for single crystal silicon nanowire

The investigation on the sensitivity of Silicon nanowire for biosensor application was done with the help of numerical simulations using the software SILVACO Atlas device simulator [23], installed in the VLSI lab of East west University. A p-type silicon nanowire was created on 500nm nitride with a 500nm buried Si layer. A secondary gate (backgate) is made with 25nm Al beneath the buried Si layer. A top gate also provided with a 2nm thick gate oxide. In the silicon nanowire, two heavily doped regions on the two sides of the channel were employed to ensure ohmic contact on the source/drain regions. The gate doping was 10^{20}/cm^{3}and the source/drain regions were also heavily doped with the doping density of 10^{20}/cm^{3}. Here, the source/drain and the channel doping were p-type. To contact source to drain and gate, aluminum electrode was chosen. This particular configuration is chosen because the fabricated biosensor that has been used to calibrate the simulator has similar configuration.

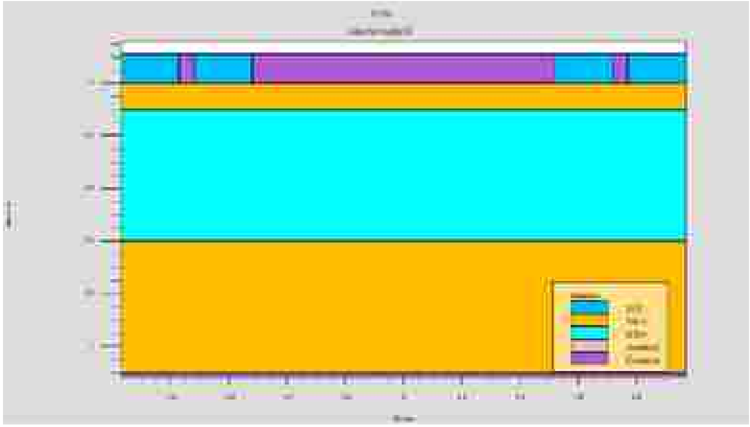

Figure 3.1: Schematic of the simulated p-type silicon nanowire.

Lombardi (CVT) model was used to take account temperature (T_L), perpendicular electric field ($E_{\perp}$), parallel electric field (E//) and doping concentration (N) effects [20]. This model surpasses any other mobility models. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by three components that are combined using Mathiessen's rule. These components are surface mobility limited by scattering with acoustic phonons(μ_{AC}), the mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b) are combined using Mathiessen's rule as follows [23]:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (3.1)$$

The first component, surface mobility limited by scattering with acoustic phonons equations [23]:

$$\mu_{AC.n} = \frac{BN.CVT}{E_{\perp}} + \frac{CN.CVT\ N^{TAU.CVT}}{T_L E_{\perp}^{\frac{1}{3}}} \quad (3.2)$$

$$\mu_{AC.p} = \frac{BP.CVT}{E_{\perp}} + \frac{CP.CVT\ N^{TAUP.CVT}}{T_L E_{\perp}^{\frac{1}{3}}} \quad (3.3)$$

The equation parameters BN.CVT, BP.CVT, CN.CVT, CP.CVT, TAUN.CVT, and TAUP.CVT used for this simulation are shown in Table 3-1[20].

The second component, surface roughness factor is given by [20]:

$$\mu_{sr} = \frac{\mathrm{DELN.CVT}}{E_{\perp}^{2}} \quad (3.4)$$

$$\mu_{sr} = \frac{\mathrm{DELP.CVT}}{E_{\perp}^{2}} \quad (3.5)$$

The equation parameters DELN.CVT and DELP.CVT used for this simulationare shown in Table 3.1 [23].

The third mobility component, mobility limited by scattering with optical intervalleyphonons is given by [23]:

$$\mu_{b.n} = \mathrm{MU0N.CVTexp}\left(\frac{-\mathrm{PCN.CVT}}{N}\right) + \frac{\left[\mathrm{MUMAXN.CVT}\left(\frac{T_L}{300}\right)^{-\mathrm{GAMN.CVT}} - \mathrm{MU0N.CVT}\right]}{1 + \left(\frac{N}{\mathrm{CRN.CVT}}\right)^{\mathrm{ALPHN.CVT}}} - \frac{\mathrm{MU1N.CVT}}{1 + \left(\frac{\mathrm{CSN.CVT}}{N}\right)^{\mathrm{BETAN.CVT}}} \quad (3.6)$$

$$\mu_{b.p} = \mathrm{MU0P.CVTexp}\left(\frac{-\mathrm{PCP.CVT}}{N}\right) + \frac{\left[\mathrm{MUMAXP.CVT}\left(\frac{T_L}{300}\right)^{-\mathrm{GAMP.CVT}} - \mathrm{MU0P.CVT}\right]}{1 + \left(\frac{N}{\mathrm{CRP.CVT}}\right)^{\mathrm{ALPHP.CVT}}} - \frac{\mathrm{MU1N.CVT}}{1 + \left(\frac{\mathrm{CSP.CVT}}{N}\right)^{\mathrm{BETAP.CVT}}} \quad (3.7)$$

Table 3.1: Parameters for Equations 3.1 to 3.8

Statement	Parameter	Default	Units
MOBILITY	BN.CVT	4.75×10^{7}	cm/ (s)
MOBILITY	BP.CVT	9.925×10^{4}	cm/ (s)
MOBILITY	CN.CVT	1.74×10^{5}	
MOBILITY	CP.CVT	8.842×10^{5}	
MOBILITY	TAUN.CVT	0.125	
MOBILITY	TAUP.CVT	0.0317	
MOBILITY	GAMN.CVT	2.5	
MOBILITY	GAMP.CVT	2.2	
MOBILITY	MUON.CVT	52.2	cm^2/ (v.s)
MOBILITY	MUOP.CVT	44.9	cm^2/ (v.s)
MOBILITY	MU1N.CVT	43.4	cm^2/ (v.s)

MOBILITY	MU1P.CVT	29.0	cm^2/ (v.s)
MOBILITY	MUMAXN.CVT	1417.0	cm^2/ (v.s)
MOBILITY	MUMAXP.CVT	470.5	cm^2/ (v.s)
MOBILITY	CRN.CVT	9.68×10^{14}	cm^{-3}
MOBILITY	CRP.CVT	2.23×10^{17}	cm^{-3}
MOBILITY	CSN.CVT	3.43×10^{20}	cm^{-3}
MOBILITY	CSP.CVT	6.10×10^{20}	cm^{-3}
MOBILITY	ALPHN.CVT	0.680	
MOBILITY	ALPHP.CVT	0.71	
MOBILITY	BETAN.CVT	2.00	
MOBILITY	BETAP.CVT	2.00	
MOBILITY	PCN.CVT	0.0	cm^{-3}
MOBILITY	PCP.CVT	0.23×10^{16}	cm^{-3}
MOBILITY	DELN.CVT	5.82×10^{14}	V/s
MOBILITY	DELP.CVT	2.054×10^{14}	V^2/s

The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) was used to reflect the recombination phenomenon within the device. The electron and hole lifetimes τ_n and τ_p were modeled as concentration dependent. The equation is given by [23]:

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (3.8)$$

$$\tau_n = \frac{TAUN0}{1+\frac{N}{(NSRHN)}} (3.9)$$

$$\tau_p = \frac{TAUP0}{1+\frac{N}{(NSRHP)}} (3.10)$$

where N is the local (total) impurity concentration. The used parameters TAUN0, TAUP0, NSRHN and NSRHP are Table 3-2 [23]. This model was activated with the CONSRH parameter of the MODELS statement.

Table 3.2: Default Parameters for Equations 3.9 to 3.11

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10^{-7}	s
METERIAL	NSRHN	5.0×10^{16}	cm^{-3}
METERIAL	TAUPO	1.0×10^{-7}	s
METERIAL	NSRHP	5.0×10^{16}	cm^{-3}

To account Bandgap narrowing effects, BGN model was used. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g, to the doping concentration, N. The expression used in ATLAS is from Slotboom and de Graaf[23]:

$$\Delta E_g = BGN.E\left\{ln\frac{\mathrm{N}}{BGN.N}+\left[\left(ln\frac{\mathrm{N}}{BGN.N}\right)^2+BGN.C\right]^{\frac{1}{2}}\right\} \quad (3.11)$$

The used values for the parameters BGN.E, BGN.N and BGN.C are shown in Table 3.3 [23].

Table 3.3: Default parameters of Slotbooms Bandgap Narrowing Model for equation 3.11

Statement	Parameter	Default	Units
MATERIAL	BGM.E	9.0×10^{-3}	v
MATERIAL	BGN.N	1.0×10^{17}	cm^{-3}
MATERIAL	BGN.C	0.5	-

3.2 Carrier Transport in Polysilicon Films

3.2.1 Electrical Properties of Polysilicon Films

A polysilicon film is composed of small crystallites joined together by grain boundaries, where the angle between the adjoining crystallites is often large. Inside each crystallite the atoms are arranged in a periodic manner which behaves like a small single crystal. The grain boundary itself is a complex structure, usually consisting of a few atomic layers of disordered atoms and a large number of defects because of incomplete atomic bonding. Several models have been proposed to explain the electrical behavior of polysilicon films. The most well-known being the competing theories of carrier trapping and segregation. In the segregation theory, it was proposed that dopant atoms can segregate to the grain boundary because of their lower energy in the disordered GB region, and therefore do not contribute to the conduction process. This would mean that the number of carriers free for conduction would be significantly less than in a, similarly doped, single crystal silicon film. The main failing of segregation theory is that it does not explain the temperature dependence of resistivity in moderately doped polysilicon films, which is thermally activated and displays a negative temperature coefficient. The competing carrier trapping theory was first proposed by Kamins [24] and then later developed into a comprehensive theory of carrier transport by Seto [25]. It has successfully explained most of the electrical properties of polysilicon for the special case where the depletion region extends throughout the entire crystallite. Baccarani*et al.* [26] published a series of results thatdemonstrated thatSeto's approximation of a monovalent trap energy level was valid. Throughout this work Seto's theory is used as the conceptual basis for explaining conduction phenomena in polysilicon.

3.2.2 Seto's Carrier Trapping Theory

It is known that there are a large number of defects due to incomplete atomic bonding at the grain boundary. These defects in the grain boundary are located where it is possible for carriers to become trapped and immobilized. This results in the traps themselves, and therefore the grain boundary becomes electrically charged. To satisfy charge neutrality an oppositely charged depletion layer of finite width forms on either side of the GB. As a consequence, the energy bands are bent at the GB creating a notch or barrier, which acts to impede carrier transport through the film. The trapping of carriers would therefore, decrease both the carrier concentration and the mobility of the material.

Carrier Trapping at Grain Boundaries

In Seto's model a number of assumptions were made to simplify his analysis.

1. The polysilicon film is composed of identical crystallites with a grain size of $L(cm)$. In a real polysilicon film there can be large variations in the size and orientation of the grains.
2. There is only one type of impurity atom present and they are full ionized and uniformly distributed with a concentration of $N(cm^{-3})$. Minority carriers and their associated traps are not considered in the analysis.
3. Inside the crystallites the single-crystal band structure of silicon is applicable. Therefore, he is assuming that the structure inside each crystallite is perfect and defect free, which is not necessarily true.
4. The grain boundary is of negligible thickness compared to the grain size L with $N_T(cm^2)$ of traps located at trap energy E_t with respect to the intrinsic Fermi level. In a real polysilicon film the traps energies are distributed across the energy gap of the band structure. Although Baccarani *et al*. **[26]**concluded that a mono-energetic approximation of the trap states was sufficient to successfully model the behavior of a polysilicon film.
5. The resulting energy band structure and charge distribution for a polysilicon film with two grain boundaries is shown in Fig. 2.1. All the mobile carriers in the region of $\left(\frac{1}{2}L - l\right) cm$ from the grain boundary are trapped by the trapping states resulting in a depletion of a potential barrier in the band structure. This analysis is considered sufficient to treat the problem in one dimension. Under this assumption Poisson's equation becomes

$$\frac{d^2V}{dx^2} = \frac{qN}{\epsilon}, l < |x| < \frac{1}{2}L(3.12)$$

where is the dielectric permittivity of polysilicon. Integrating equation (2.1) twice and applying the boundary conditions that $V(x)$ is continuous and $\frac{dV}{dx} = 0$ when $x = l$ gives us

$$V(x) = \frac{qN}{2\epsilon}(x - l)^2 + V_{VO}, l < |x| < \frac{1}{2}(3.13)$$

where is the potential of the valence band edge at the center of the crystallite. Throughout the calculation the intrinsic Fermi level is taken to be at zero energy, which is positive towards the valence band.

There are two cases that we need to consider that are related to the doping concentration.

1. $N < \frac{N_T}{L}$ and
2. $N > \frac{N_T}{L}$

where we define a critical doping concentration $N^* = \frac{N_T}{L}$

Below critical doping concentration $< \frac{N_T}{L}$

Considering first of all the case when $< \frac{N_T}{L}$. This condition implies that the crystallite is completely depleted of carriers and the traps are partially filled so that and (2.2) becomes

$$V(x) = V_{VO} + \frac{qN}{2\epsilon}x^2 \qquad (3.14)$$

The potential barrier height V_B is the difference between $V(0)$ and $V\left(\frac{1}{2}L\right)$, therefore

$$V_B = \frac{qL^2N}{8\epsilon}, N < \frac{N_T}{L} (3.15)$$

Above the critical doping concentration $> \frac{N_T}{L}$

In Seto's model the energy of the grain boundary traps is assumed to be sodeep that they are completely filled when the dopant concentration exceeds the critical value $N^* = \frac{N_T}{L}$. As we increase the dopant concentration above this value, the number of trapped carriers remains constant at the value, and the added carriers act to form neutral regions within the grains, as seen in Fig. 2.2. This reduces the depletion region width, but to satisfy charge neutrality the value of charge in the depletion region remains constant, albeit in a smaller area. This results in the potential barrier height receding. The width of the depletion region decreases according to the relation

$$x_d = \frac{N_T}{2N} \qquad (3.16)$$

Therefore the barrier height when $N > \frac{N_T}{L}$ is found to be

$$V_B = \frac{qN}{2\epsilon}x_d^2 = \frac{qN}{2\epsilon}\left(\frac{N_T}{2N}\right)^2 = \frac{qN_T^2}{8\epsilon N} \qquad (3.17)$$

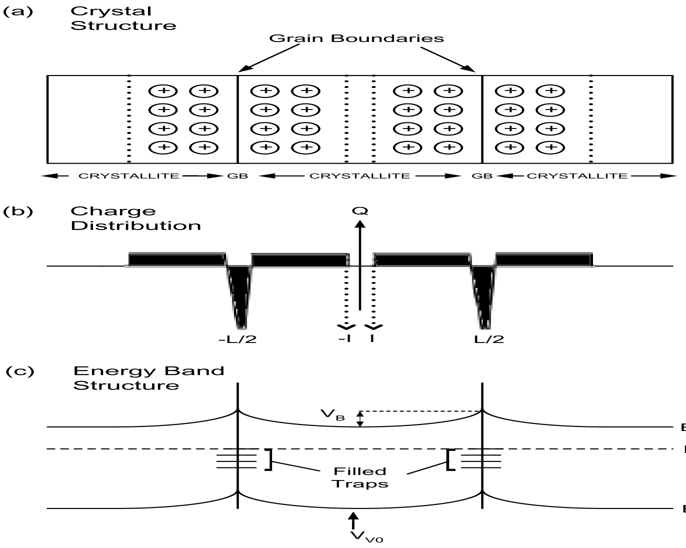

Figure 3.2: (a) The simplified model of the crystallite structure in the polysilicon film showing a single crystallite separated from the two adjoining crystallites by grain boundaries (b) The charge distribution in the structure, showing the negatively charged GB and the surrounding positively charged depletion layer (c) Energy band structure with potential barriers forming at the grain boundaries.

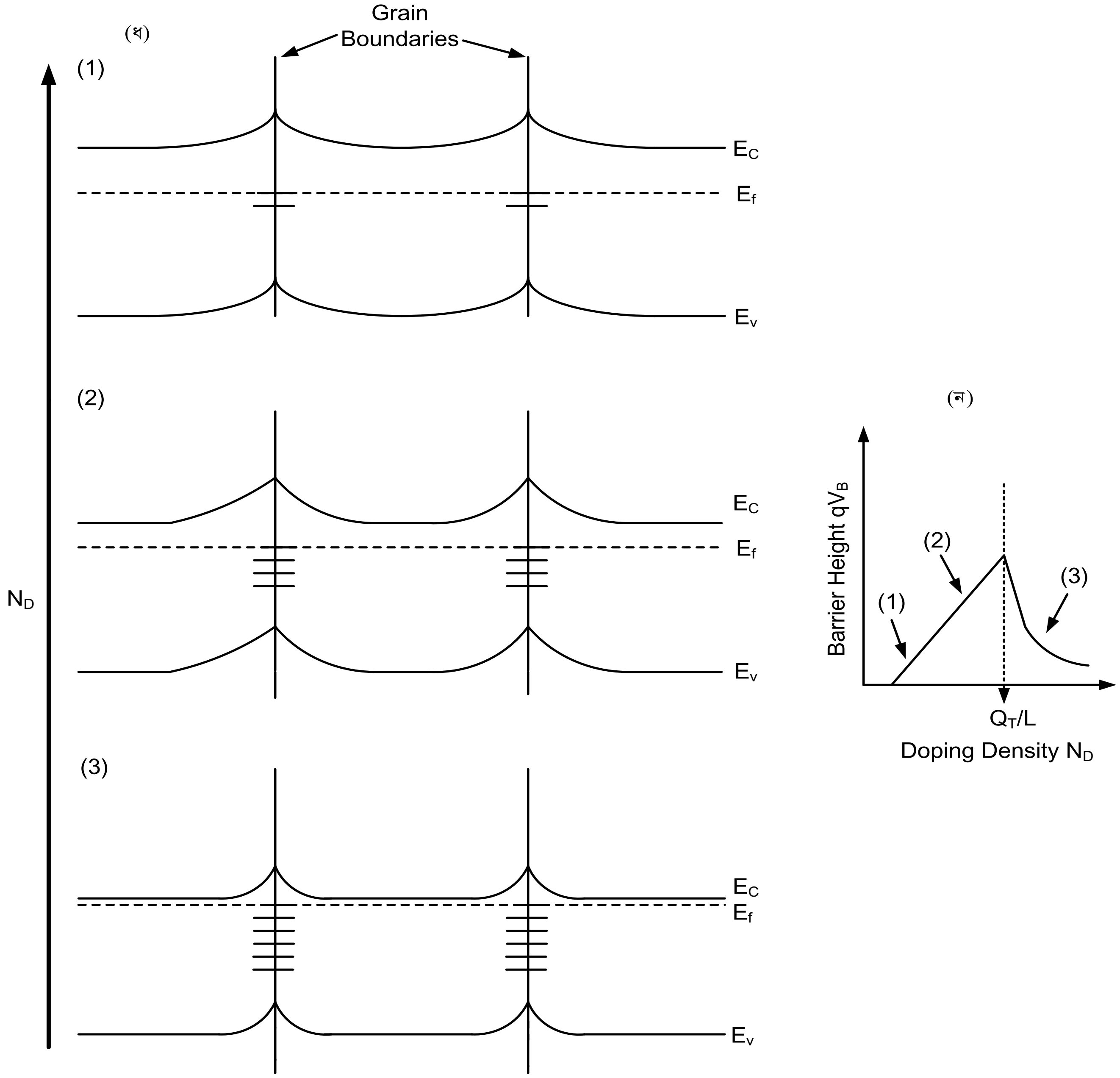

Figure 3.3: (a) As the doping density is increased, the trap states at the grain boundary become filled, increasing the barrier height. When the doping density is increased beyond the critical value N^*, the free carriers reduce the depletion width and the barrier height recedes, (b) barrier height increases linearly as a function of N until reaching the critical value, beyond which it decreases rapidly as a function of $\boldsymbol{1/N}$.

Thus, as shown in Fig. 3.3 as the dopant concentration is increased in the film, firstly the potential barrier increases as a function of, and then above the critical doping concentration it decreases rapidly as a function of $\frac{1}{N}$.

3.2.3 Transport calculation of polysilicon Films

It is assumed that carrier transport, in moderately doped polysilicon films, is dominated by thermionic transport over the barriers. At moderate doping concentration of around 1×10^{17} cm^{-3} the barrier width is still tens of nanometers wide for tunnellingto be significant. At high doping concentrations, the barrier is narrow enough to allowtunneling to contribute to the current flow.

The thermionic-emission current density Jcan be written as

$$J = qnv_c ex\,p\left[-\frac{q}{kT}(V_B - V)\right] \qquad (3.18)$$

where is the free-carrier density $v_c = \sqrt{\frac{k\mathrm{T}}{2\pi m^*}}$, is the collection velocity V_B, is the barrier height with no applied bias, and is the applied bias across the depletion region.

Under an applied bias the current flow in one direction increases while carrier transport in the other direction decreases. Therefore, we must consider current flow in both the forward and reverse directions. The net current density given by $J = J_F - J_R$. With $V \approx \frac{1}{2}V_G$, where V_G is the bias across one grain boundary.

$$J_F = qnv_c ex\,p\left[-\frac{q}{kT}\left(V_B - \frac{1}{2}V_G\right)\right] \qquad (3.19)$$

$$J_R = qnv_c ex\,p\left[-\frac{q}{kT}\left(V_B - \frac{1}{2}V_G\right)\right] \qquad (3.20)$$

The net current density under applied bias then becomes

$$J = qnv_c ex\,p\left[-\frac{qV_B}{kT}\right]\left[exp\left(\frac{qV_G}{2kT}\right) - exp\left(-\frac{qV_G}{2kT}\right)\right] \quad (3.21)$$

$$J = 2qnv_c exp\left(-\frac{qV_B}{kT}\right)sinh\left(\frac{qV_G}{2kT}\right) \qquad (3.22)$$

We can obtain a linear relationship between current and applied voltage if we make the following simplification for low applied voltages

$$sinh\left(\frac{qV_G}{2kT}\right) \approx \left(\frac{qV_G}{2\mathrm{k}T}\right) \qquad (3.23)$$

Therefore

$$J = \frac{q^2 nv_c}{kT}\left[exp\left(-\frac{qV_B}{kT}\right)\right]V_G \qquad (3.24)$$

We can now obtain an expression for the conduction $\sigma = \frac{J}{\epsilon} = \frac{JL}{V_G}$

$$\sigma = \frac{q^2 nv_c L}{kT} exp\left(-\frac{qV_B}{kT}\right) \qquad (3.25)$$

Thus condition in polysilicon is an activated process with activation energy of approximately, which depends on the dopant concentration and the grain size. Many analytical models of polysilicon nanowire operation in the subthreshold and turn-on regions have been developed based on Seto's theory [27-31]. So far we have developed an analytical model that is valid in one dimension. However, in short channel field effect transistors, a two dimensional analysis is necessary to adequately describe the device operation. Therefore, we need to use 2D numerical device simulation to realistically study the effect of the GB, in short channel polysilicon nanowires.

3.2.4 Numerical Simulation of Polysilicon Devices

The trend in the semiconductor industry towards MOSFETs of ever decreasing gate lengths has increased the demand for accurate numerical device simulation technologies. As devices enter the sub-micron regime, complex 2D effects begin to determine the device behavior in the subthreshold regime, and therefore, 2D device simulation is needed to provide insight and predictive analysis. The classical Drift-Diffusion model (DD) has been extensively studied for almost forty years, since Gummel*et al.* [32] reported on the one-dimensional numerical simulation of a silicon bipolar transistor. Even as the MOSFET enters the deca-nanometer regime, where ballistic and quantum mechanical effects can play significant roles in carrier transport, DD modeling is still one of the most practical and powerful tools in FET design. With some modifications (such as the inclusion of momentum and energy balance equations) it can still provide reasonable accuracy and importantly great computational efficiency, compared to more elaborate techniques, such as practical based ensemble Monte-Carlo simulations.

In our simulation studies of the device, we use commercial simulator ATLAS [23] from SILVACO international. ATLAS uses the basic device modeling equation for DD modeling. The basic semiconductor equation begins with Poisson's equation that describes the relationship between the electrostatic potential ψ to the space charge density ρ

where is the local permittivity. $\nabla.(\varepsilon\nabla\psi) = -\rho(3.26)$

The carrier continuity equation for both electrons and holes are defined in terms of the current densities $\vec{J_n}, \vec{J_p}$ and the generation and recombination rates for electrons and holes (G_n, $G_p$and R_n, R_p) respectively.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.\vec{J_n} + G_n - R_n \qquad (3.27)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla.\vec{J_p} + G_p - R_p \qquad (3.28)$$

The electron and hole current densities $\vec{J_n}$ and$\vec{J_p}$ are then expressed in terms of their respective quasi-Fermi potentials ϕ_n andϕ_p.

$$\vec{J_n} = -q\mu_n \nabla\phi_n \qquad (3.29)$$

$$\vec{J_p} = -q\mu_p \nabla\phi_\mathrm{p} \qquad (3.30)$$

where μ_n and μ_p are the electron and hole mobilities respectively.

The carrier concentration are expressed in the following quasi-Boltzmann form in terms of both quasi-fermi potentials ϕ_n and ϕ_p and the intrinsic potential ψ

$$n = n_i exp\left[\frac{\psi - \phi_n}{V_T}\right] \qquad (3.31)$$

$$p = n_i exp\left[\frac{\psi - \phi_p}{V_T}\right] \qquad (3.32)$$

where V_T is the thermal voltage ($V_T = k_B T/q$) and n_i is the intrinsic carrier concentration.

3.2.5 Modeling Deep Trap Emission and Absorption with Shockley-Read-Hall Statistics

We now include the carrier trapping mechanisms, via the deep trap states at the grain boundary. The model used was originally developed for carrier emission-absorption processes from the donors and acceptors in heterojunction structures [33-34]. However, it is equally applicable to silicon devices. By using the derived expressions, we then modify the basic device transport equations accordingly.

We start by defining two types of trap that exchange charge with the conduction and valance bands through the emission and recombination of electrons. At the grain boundary, these would exist in the forbidden energy gap as a result of incomplete or dangling bonds in the semiconductor lattice.

Firstly we define donor-like traps as positively charged when empty and neutral when filled by electron. Secondly, we define acceptor-like traps to be negative when filled by an electron but otherwise neutral. Therefore, traps above the Fermi-level are acceptor-like and those below are donor-like. This is illustrated along with the possible capture and emission processes in Fig 3.4.

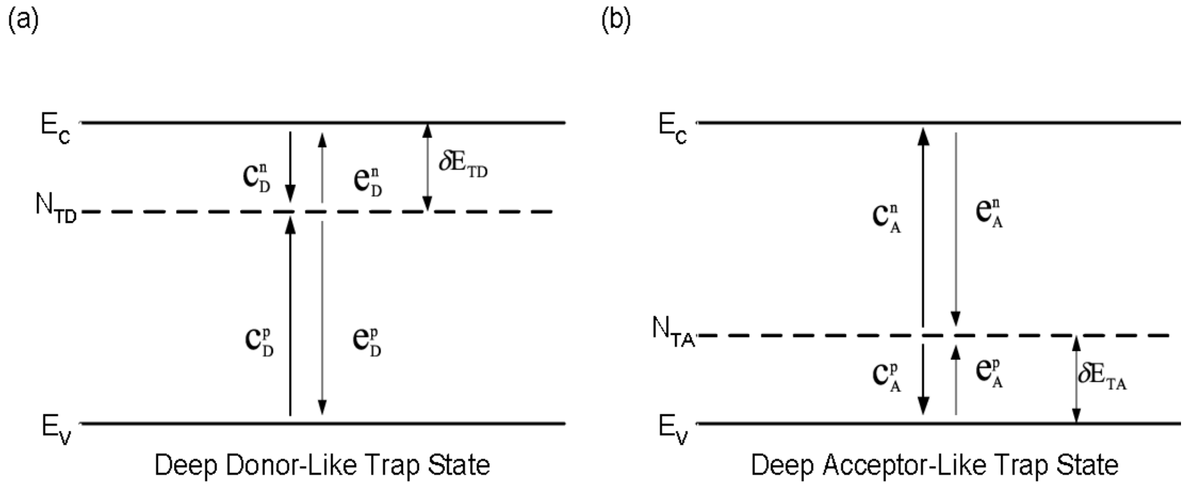

Figure 3.4: An illustration of the possible capture and emission processes from trap states deep in the energy band gap for (a) donor-like traps and (b) acceptor-like traps.

The energies of donor-like (E_{TD}) and acceptor-like (E_{TA}) traps are expressed as

$$\Delta E_{TA} = \psi + E_C - \delta E_{TA} \qquad (3.33)$$

$$\Delta E_{TD} = \psi + E_V - \delta E_{TD} \qquad (3.34)$$

The time evolution of the density of carriers at the deep levels is given by the following rate equations [35];

$$\frac{\partial}{\partial t}(N_{TD}-N_{TD}^{+}) = C_D^n N_{TD}^{+} n - e_D^n (N_{TD}-N_{TD}^{+})$$

$$-C_D^p (N_{TD}-N_{TD}^{+}) p - e_D^p N_{TD}^{+} \qquad (3.35)$$

$$\frac{\partial}{\partial t}(N_{TA}-N_{TA}^{-}) = C_A^p N_{TA}^{-} p - e_A^p (N_{TA}-N_{TA}^{-})$$

$$-C_A^n (N_{TA}-N_{TA}^{-}) n - e_A^n N_{TA}^{-} \qquad (3.36)$$

where the carrier emission rates $^{n}_{D}$, e_D^p, e_A^n, e_A^p are related to the carrier capture rates C_D^n, C_D^p, C_A^n, C_A^p by the relations;

$$e_D^n = C_D^n n_1^D \qquad (3.37)$$

$$e_D^p = C_D^p p_1^D \qquad (3.38)$$

$$e_A^n = C_A^n n_1^A \qquad (3.39)$$

$$e_A^p = C_A^p p_1^A \qquad (3.40)$$

where $^{D}_{1}$,p_1^D, n_1^A, p_1^A are given by the following;

$$n_1^D = n_i g_D exp\left[\frac{\Delta \mathrm{E}_{TD}}{k_B T/q}\right] (3.41)$$

$$p_1^D = n_i g_D exp\left[\frac{-\Delta E_{TD}}{k_B T/q}\right] (3.42)$$

$$n_1^A = n_i g_A exp\left[\frac{\Delta E_{TA}}{k_B T/q}\right] (3.43)$$

$$p_1^A = n_i g_A exp\left[\frac{-\Delta E_{TA}}{k_B T/q}\right] (3.44)$$

In Eq. 3.41-3.44 g_D and g_A are the degeneracies of the deep donor-like and acceptor-like trap states. A steady state-solution for the concentration of trapped charge at the GB can found from the Eq. 2.24 and 2.25. This gives us;

$$N_{TD}^{+} = \frac{n_1^D/C_D^p + p/C_D^n}{(n+n_1^D)/C_D^p + (p+p_1^D)/C_D^n} N_{TD} (3.45)$$

$$N_{TA}^{-} = \frac{n_1^A/C_A^p + p/C_A^n}{(n+n_1^A)/C_A^p + (p+p_1^A)/C_A^n} N_{TA} (3.46)$$

The additional charge at the grain boundary alters the electrostatic potential by appearing as additional charge terms on the right hand side of Poisson’s equation. So Eq. 3.26 then becomes;

$$\nabla.(\varepsilon \nabla \psi) = -q(N_D^{+} + N_{TD}^{+} - N_A^{-} - N_{TA}^{-} - n + \mathrm{p}) \qquad (3.47)$$

where N_D^+ and N_A^- are the concentrations of ionized shallow donors and acceptors.
In addition, there is induced electron-hole recombination, and therefore there is a change in the current distribution through an additional generation/recombination terms on the right hand side of Eq. 2.16 and 3.28. This gives us the following expressions;

$$q\frac{\partial n}{\partial t} = \nabla.\overrightarrow{J_n} + G + R - C_D^n N_{TD}^+ n - e_D^n (N_{TD} - N_{TD}^+) \qquad - C_A^n (N_{TA} - N_{TA}^-) n - e_A^n N_{TA}^- (3.48)$$

$$q\frac{\partial p}{\partial t} = \nabla.\overrightarrow{J_p} + G + R - C_A^p\ (N_{TD} - N_{TD}^+) p \qquad - e_A^p N_{TD}^+ - C_A^p N_{TA}^- n - e_{\mathrm{A}}^p (N_{TA} - N_{TA}^-) (3.49)$$

where, G and R are the conventional semiconductor generation and recombination terms respectively. If we solve for the steady state (i.e. $\frac{\partial n}{\partial t} = 0$ and $\frac{\partial p}{\partial t} = 0$) then the Eq. 3.48 and 3.49 reduce to the following current continuity equations;

$$\nabla.J_n = -(G - R - R_{TD} - R_{TA}) \qquad (3.50)$$

$$\nabla.J_p = (G - R - R_{TD} - R_{TA}) \qquad (3.51)$$

where R_{TD} and R_{TA} are the recombination rates through the donor-like and acceptor-like trap states and are given by;

$$R_{TD} = \frac{np - n_1^D p_1^D}{(n + n_1^D)/C_D^p + (p + p_1^D)/C_D^n} N_{DD} (3.52)$$

$$R_{TA} = \frac{np - n_1^A p_1^A}{(n + n_1^A)/C_A^p + (p + p_1^A)/C_A^n} N_{DA} \qquad (3.53)$$

The expression given by Eq. 3.50-3.53 are discretised onto a two-dimensional finite difference mesh lattice and then numerically solved in an iterative way using the standard Gummel's scheme [33,36].

3.2.6 Continuous Trap-State Density Distribution Model

So far we have assumed that the acceptor-like and donor-like trap states are mono-energetic; that is, they exist at only one energy level in the forbidden gap. For a more accurate simulation, a continuum of trap states distributed across the energy band gap can be defined, using the commercial device simulator ATLAS. To do this, we again modify the space charge term Q_T representing trapped charge. This is given by

$$-p = q(p - n + N_D^+ - N_A^-) + Q_T \qquad (3.54)$$

$$Q_T = q(p_T - n_T) \qquad (3.55)$$

where, N_D^+ and N_A^- are the ionized donor and acceptor concentrations respectively and p_T and n_T are the trapped hole and electron concentrations respectively.

Again we assume that the trap states consist of both donor-like and acceptor-like states, distributed across the forbidden energy gap. We can write the total density of states as

$$g(E) = g_D(E) + g_A(E) \qquad (3.56)$$

where $g_D(E)$ is the total density of donor-like trap states and $g_A(E)$ is the total density of acceptor-like trap states. Attempts to experimentally measure the continuum of trap states at the grain boundary in Polysilicon films, suggest that both, donor-like and acceptor-like states, consist of two components. Firstly, an exponential Tail distribution which intercepts the adjacent energy band at its maximum value and decays rapidly toward the centre ($g_{TA}(E)$ for acceptor and $g_{TD}(E)$ for donors). Secondly a Gaussian distribution of traps located deep in the energy gap ($g_{GA}(E)$ for acceptors and g_{GD} for donors). These terms are expressed as:

$$g_{TA}(E) = N_{TA} exp\left[\frac{E - E_C}{W_{TA}}\right] \qquad (3.57)$$

$$g_{TD}(E) = N_{TD} exp\left[\frac{E - E_C}{W_{TD}}\right] \qquad (3.58)$$

$$g_{GA}(E) = N_{GA} exp\left[-\left[\frac{E_{GA} - E}{W_{GA}}\right]^2\right] \qquad (3.59)$$

$$g_{GD}(E) = N_{GD} exp\left[-\left[\frac{E_{GD} - E}{W_{GD}}\right]^2\right] \qquad (3.60)$$

where N_{TA} and N_{TD} are the trap state densities at the point of intercept with the conduction band (acceptor-like) and valence band (donor-like) respectively and W_{TA}, W_{TD} are the characteristic decay energies. For the Gaussian type states N_{GA} and N_{GD} are the total density of trap states; W_{GA} and W_{GD} are the characteristic decay energies defining the spread of the Gaussian and finally, E_{GA} and E_{GD} are the position of the Gaussian peaks in the energy band gap. All quantities are for acceptor-like and donor-like trap respectively as denoted in the subscript. For clarification, the role of these quantities is illustrated by the example distribution shown in Fig. 3.5.

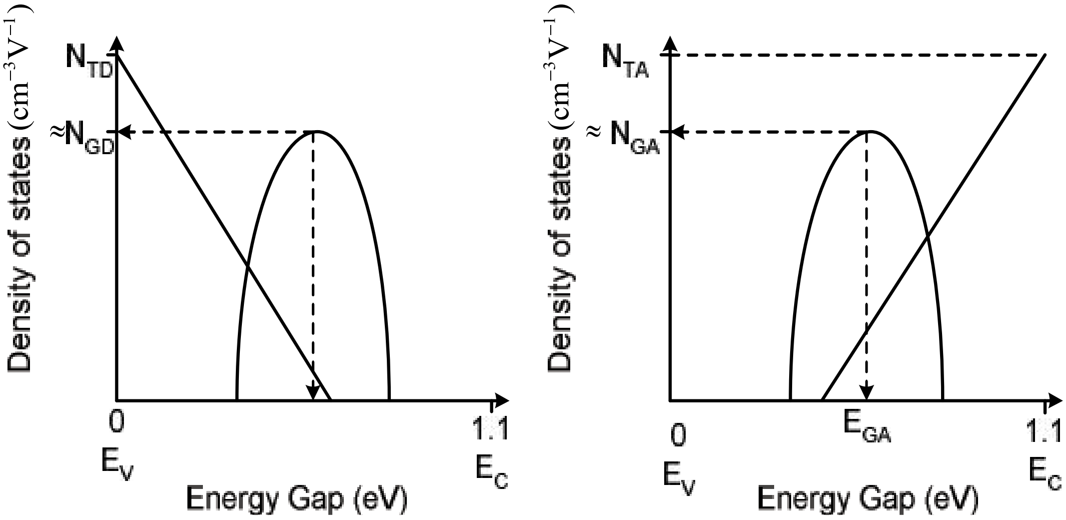

Figure 3.5: An illustration of a possible (a) acceptor-like and (b) donor-like distribution of trap states across the energy band gap and how they relate to the model parameters.

$$n_T = \int_{E_V}^{E_C} g_A(E) f_A(E, n, p)\, dE \qquad (3.61)$$

$$p_T = \int_{E_V}^{E_C} g_D(E) f_D(E, n, p)\, dE \qquad (3.62)$$

To calculate the trapped charge we perform a numerical integration of the product of the trap density and its occupation probability over the forbidden energy gap. This gives

for trapped electrons and hole respectively, where f_A and f_D are the occupation probability for acceptor-like and donor-like traps.

If we then assume that the capture cross section for Gaussian and Tail states are equal, then the occupation probabilities are then given by

$$f_A = \frac{v_n \sigma_{ae} n + v_p \sigma_{ah} p_t}{v_n \sigma_{ae}(n + n_t) + v_p \sigma_{ah}(p + p_t)} \qquad (3.63)$$

$$f_D = \frac{v_n \sigma_{de} n + v_p \sigma_{dh} p_t}{v_n \sigma_{de}(n + n_t) + v_p \sigma_{dh}(p + p_t)} \qquad (3.64)$$

Where σ_{ae},σ_{ah}andσ_{de},σ_{dh} are the electron and hole capture cross sections for acceptor-like and donor-like traps respectively. The effective electron and hole concentrations $n_t$and p_t are defined as

$$p_t = n_i exp\left[\frac{E_i - E}{kT}\right] \qquad (3.65)$$

$$n_t = n_i exp\left[\frac{E - E_i}{kT}\right] \qquad (3.66)$$

where n_i, is the intrinsic carrier concentration, E is the trap energy level, E_i is the intrinsic fermi level and T is the lattice temperature.

The Shockley-Read-Hall recombination/generation rate [35, 37] per unit time is modified to include the multiple trap levels and is given by;

$$U_{n,p} = \int_{E_V}^{E_C} \left(\frac{v\ \ v_p \sigma_{ae} \sigma_{ah} \left(np - n_i^2\right) g_A(E)}{v_n \sigma_{ae}(n + n_t) + v_p \sigma_{ah}(p + p_t)} + \frac{v_n v_p \sigma_{de} \sigma_{dh}(np - n_i^2) g_D(E)}{v_n \sigma_{de}(n + n_t) + v_p \sigma_{dh}(p + p_t)} \right) dE \qquad (3.67)$$

3.3 Simulation of poly silicon nanowire

The 2D coupled Poisson's drift-diffusion solver with Fermi-Dirac (FERMI) carrier statistics was also used to model carrier transport in poly silicon NW. We used constant mobility model for polysilicon NWs simulation because TFT module in ATLAS is compatible with constant low field mobility model only. Use of other mobility model overwrites constant low field model and gives inaccurate results. Constant low field mobility model is independent of doping concentration, carrier densities and electric field. It does account for lattice scattering due to temperature according to:

$$\mu_{n0} = MUN\left(\frac{T_L}{300}\right)^{-TMUN} \qquad (3.68)$$

$$\mu_{p0} = MUP\left(\frac{T_L}{300}\right)^{-TMUP} \qquad (3.69)$$

where T is the lattice temperature. The low field mobility parameters: MUN, MUP, TMUN and TMUP can be specified in the MOBILITY statement with the defaults as shown in Table 3.4.

Table 3.4: Default mobility model values for polysilicon

Statement	Parameter	Defaults	Unit
MOBILITY	MUN	1000	cm^2/ V.s
MOBILITY	MUP	500	cm^2/ V.s
MOBILITY	TMUN	1.5	-
MOBILITY	TMUP	1.5	-

However, we have used MUN=14 cm^2/ V.s and MUP=6 cm^2/ V.s as experimentally extracted mobility of similar polysilicon nanowires within the range of 6 cm^2/ V.s to 12 cm^2/ V.s considering variation of polysilicon nanowire width and height after fabrication [10].

Fermi-Dirac (FERMI) carrier statistics model was used to account for certain properties of very highly doped (degenerate) materials.In this model the probability $f(\varepsilon)$ that an available electron state with energy ε is occupied by an electron is**:**

$$f(\varepsilon) = \frac{1}{1 + exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \qquad (3.70)$$

where E_F is a spatially independent reference energy known as the Fermi level and k is Boltzmann'sconstant. In the limit that $\varepsilon - E_F >> kT_L$E Equation (3.3) can be approximated as:

$$f(\varepsilon) = exp\left(\frac{E_F - \varepsilon}{kT_L}\right) (3.71)$$

Statistics based on the use of equation (3.71) are referred to as Boltzmann statistics. The use of Boltzmann statistics instead of Fermi-Dirac statistics [35-39] makes subsequent calculations much simpler. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. In ATLAS we used Fermi-Dirac statistics by specifying the parameter FERMIDIRAC on the MODEL statement.

The Shockley-Read-Hall (SRH) model was used for recombination phenomenon within the device. The carrier emission and absorption process (or Phonon transitions) occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. The theory of two steps process was first proposed by Shockley and Read [35] and then by Hall [37]. The Shockley-Read-Hall recombination is modeled as follows:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO\left[n + n_{ie} exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUNO\left[p + n_{ie} exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (3.72)$$

where *ETRAP* is the difference between the trap energy level and the intrinsic Fermi level, T_L is the lattice temperature in degrees Kelvin and *TAUNO* and *TAUPO* are the electron and hole lifetimes. This model is activated with the SRH parameter of the MODELS statement. The electron and the hole lifetime parameters *TAUNO* and *TAUPO* are user definable on the MATERIAL statement. The default values for carrier lifetimes are shown in Table 3.5. Materials other than silicon will have different defaults and full descriptions of these are given in Table 3.6.

Table 3.5: Default parameters for equation 3

Statement	Parameter	Defaults	Units
MATERIAL	ETRAP	0	V
MATERIAL	TAUNO	1.0×10^{-7}	s
MATERIAL	TAUPO	1.0×10^{-7}	s

Table 3.6: Default parameters of polysilicon recombination parameters

Material	TAUNO (s)	TAUPO (s)	NSRHN (cm^{-3})	NSRHP (cm^{-3})
Polysilicon	1.0×10^{-7}	1.0×10^{-7}	5.0×10^{16}	5.0×10^{16}

To account bandgap narrowing effects, BGN model was used. In the presence of heavy doping, greater than $10^{18}cm^{-3}$, experimental work has shown that the pn product in silicon becomes doping dependent [40]. As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. In ATLAS this is simulated by a spatially varying intrinsic concentration n_{ie} defined according to the equation 3.6:

$$n_{ie}^2 = n_i^2 \left(\frac{\Delta E_g}{kT}\right) \quad (3.73)$$

Bandgap narrowing effects in ATLAS are enabled by specifying the BGN parameter of the MODELS statement. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g to the doping concentration, *N*. The expression used in ATLAS is from Slotboom and de Graaf [41]:

$$\Delta E_g = BGN.E\left\{ln\frac{N}{BGN.N} + \left[\left(ln\frac{N}{BGN.N}\right)^2 + BGN.C\right]^{\frac{1}{2}}\right\} \quad (3.74)$$

The parametersand may be user defined on the MATERIAL statement and have the defaults shown in Table 3.5.

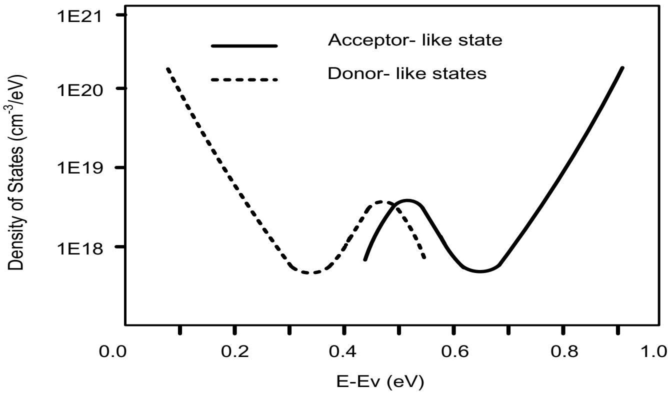

Figure 3.6: The distribution of acceptor and donor-like trap states across forbidden energy gap.

Polysilicon is a disorder material which contains a large number of defects states within the band gap of the material and interface. To accurately simulate the polysilicon NWs with defects in ATLAS; the continuous defect density of states (DOS) used. The defect states as a combination of exponentially decaying band Tail states and Gaussian distribution of mid gap states [42-43] shown in Fig. 3.2 which theory described in chapter 2. In our work we have used continuous defect density of states (DOS) for p-type polysilicon nanowire simulation.

In polysilicon devices interface trap levels capture carriers, which slow down the switching speed of any device. The capture cross sections are used to define the properties of each trap. In ATLAS the INTTRAP command activates interface defect traps at discrete energy levels within the bandgap of the semiconductor shown in Fig. 3.7. We used discrete interface trap levels for simulation as it significantly reduces run time.

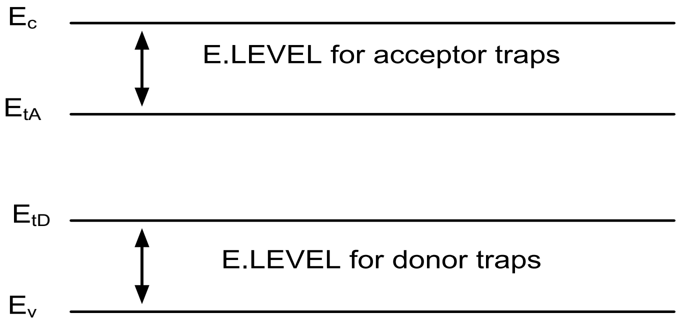

Figure 3.7: The trap energy level for acceptor and donor-like traps in reference of conduction and valance band edges.

3.4 Simulation profile

Device simulation using silvaco atlas usually faces convergence problems and necessitates a long simulation run times. To avoid these problems, the simulation of silicon nanowire MOSFET has been divided into a few groups. At first, structure definition was performed. In this definition the simulation focused on creating the structure with a suitable mesh density. Regions and electrodes were defined as depicted in Figure 3.8. Finer nodes were assigned in critical areas, such as across the gate oxide to monitor channel activity and to get a better picture of the depletion layer and junction behavior near the source/drain boundaries. A coarser mesh was used elsewhere in order to reduce simulation run time.

Once the structure and the mesh were found to be as desired, the simulation was performed with appropriate models as discussed in section 2.1 and numerical solving methods. The model was invoked by using the statements FERMI, CVI, CONSRH, BGN. The numerical solving methods GUMMEL, NEWTON were used to reduce the simulation run time, while keeping the accuracy of the simulation at an acceptable level.

To get convergence, a special bias point solving method was used. It was found that the simulation faced difficulty in solving the initial desired bias points i.e. ±1V, ±2V, ±3V, ±4V, ±5V for back gate voltage ±1V for drain voltage. Therefore, the initial gate bias was set to 0.005V and the next bias point was set to 0.05V, before finally setting the bias point to desired value.

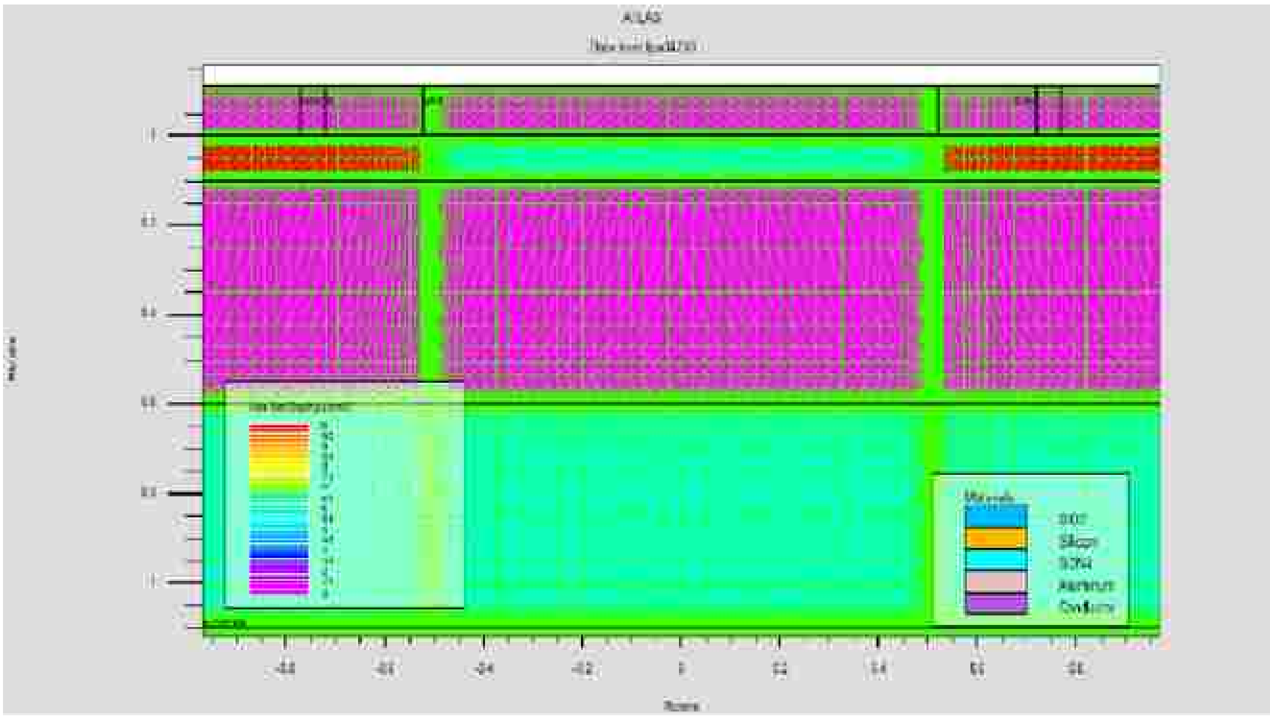

Figure 3.8: Cross-sectional view of p-type nanowire showing the mesh density used in this simulation.

CHAPTER 4

4. CALIBRATION OF THE TCAD SIMULATOR

This chapter describes the calibration of the SILVACO simulator with experimental results supplied from Southampton Nanofabrication Center. The available experimental characteristics are for 10 µm long polysilicon nanowires with a p-type body doping $6 \times 10^{16}/cm^3$ and the nanowires have cross sectional dimensions of (100 nm × 100 nm) on nitride platform,which is described in chapter 3 (Fig. 3.1). Single crystal silicon model in SILVACO is pretty standard which has been used to simulate the characteristics of single crystal silicon devices for many years. The polysilicon is modeled using continuous trap states (both donor-like and acceptor-like)distribution across the energy band gap. However, the parameters of the trap states depend on the polysliconprocessing conditions and hence, these parameters are calibrated using the polysilicon nanowires' experimental data. Once the device platform (Fig. 3.1) with polysilicon nanowires are calibrated with the experiment, the polysilicon material is replaced with single crystal silicon material while keeping interface states same as before by deactivating the continuous trap states inside the silicon that is used to represent polysilicon material. This allowed us accurate simulation of both polysilicon and single crystal silicon nanowires in same platform like buried layer, supporting base wafer, top oxide layer and same condition of interface states. This interface states, which is extracted from experiment, corresponds to Si/SiO_2 intrinsic interface states without any contribution from grain boundaries.

It is worth noting at this point that to accurately predict material effect, NW simulation for different types of silicon should be done in a same device platform as same NW in different platform will exhibit different characteristics due to different distribution of electric fields. Direct calibration of the single crystal Si NW on nitride was not attempted due to unavailability of experimental results of single crystal Si NWs on nitride platform and also due to the unavailability of NWs with same dimensions/doping. However, calibration of polysilicon NW on nitride platform and switching polysilicon with single crystal silicon is accurate as single crystal silicon parameters that are used in SILVACO, which is pretty standard and has been used to simulate the characteristics of single crystal silicon devices for many years. The unknown interface states for single crystal silicon NWs are extracted from polysilicon NW simulation and used.

Physical understanding of the effect of different types of grain boundary defects and interface states (donor and acceptor types) and their distribution profile on the electrical behavior of the p-type polysilicon NW is achieved by investigating each type of defects individually. This knowledge is used to calibrate experimental p-type polysilicon NWs electrical characteristics to find out the types and order of the defects that can be expected in p-type polysilicon NW biosensors if fabricated by deposition and etch technique.

4.1 Polysilicon Nanowire without Defect

The p-type polysilicon device is like a single crystal Si device without considering any defect of the material. This section shows the p-type polysilicon nanowire electrical characteristics without any defect of the material.

The Fig. 4.1 shows subthreshold characteristics of the p-type polysilicon NWs without any grain boundaries or interface states. Thecurve illustrated for different drain voltage without considering any defects while using Si underneath the nitride as back-gate. The reason for such simulation is that the experimental data is available at this condition.

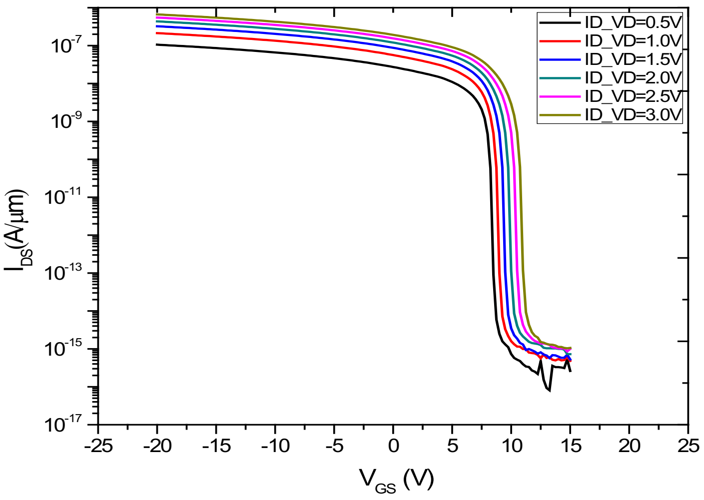

Figure 4.1: I_{DS}-V_{GS} (Log Scale) of p-type polysilicon NWs without considering material defects.

No significant degradation of subthreshold slope is observed with increasing drain bias with values of 181.72 mV/decade to 183.80 mV/decade for applied drain voltage of 0.5 V to 3.0 V. This result does not explain the results of the fabricated p-type polysilicon nanowire as reported in [31] where subthreshold slopes are around 2.3-3.0 V/decade.

To investigate the reason behind the degraded p-type polysilicon, nanowire characteristics are introduced in NWs by incorporating different types of defects in simulation.

4.2 Effect of Interface Trap States

Interface states are usually created during nanowire fabrication because of the generation of surface roughness during dry etch and also due to the lattice mismatch between two material interfaces. The nanowire device under consideration has a nitride layer underneath it. In addition, a 10 nm oxide layer was grown on the top of the nanowire by oxidation for biomolecule attachment through silanization. As a result, accumulations of interface states are expected in these nanowires. However, literature supports that depending on the process conditions interface states may capture positive or negative charges. The type of charges in our considered nanowire is not known and hence, we first study the effect of both types of interface states for p-type polysilicon understanding and for calibration.

4.2.1 Effect of Acceptor-like Interface Trap States

To study the effect of acceptor-like interface states, acceptor like states are created between the polysilicon and silicon-dioxide layer and also between the polysilicon and nitride layer underneath the nanowire. The densities of acceptor-like interface states are varied from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}. Fig. 4.2 shows p-type polysilicon nanowires subthreshold characteristics at different values of acceptor like interface states for a drain bias of 0.5V. During this measurement, n-type silicon region underneath the nanowire and nitride was used as gate.

It is observed that variation of acceptor-like interface trap density affects neither drive current nor the subthreshold characteristic. However, it can be seen that acceptor like interface states significantly affect the leakage current of the device. Here Leakage current is increased from 3.87×10^{-16} A/µm to 4.86×10^{-13} A/µm as the density of the acceptor state is increased from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}.

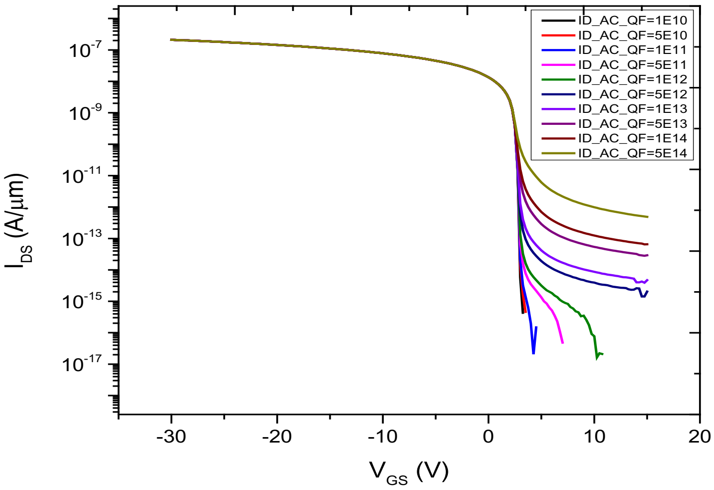

Figure 4.2: Effect of acceptor-like interface trap states.

4.2.2 Effect of Donor-like Interface Trap States

Fig. 4.3 shows p-type polysilicon nanowires subthreshold characteristics at different values of donor like interface states for a drain bias of 0.5V. During this measurement n-type silicon region underneath the nanowire and nitride was used as gate. It can be seen that the variation of donor-like interface states does not affect the leakage current at all. However, it can be seen that donor-like interface states significantly affects drive current and the subthreshold characteristic.

The sub-threshold slope increases from 158.95 mV/decade to 3.79 V/decade for an increase of density of donor like interface states from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}. Similarly the drive current decrease from 2.07×10^{-7} A/µm to 1.55×10^{-14} A/µm as donor density increases from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}.

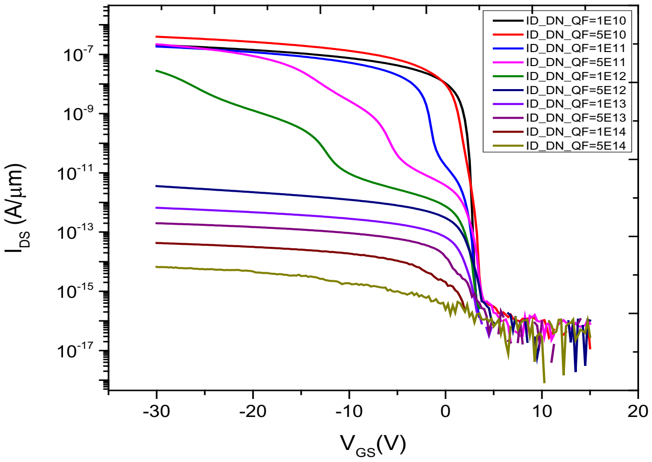

Figure 4.3: Effect of donor-like interface trap states.

4.3 Effect of Grain Boundary / Trap States in Polysilicon Channel Region

Polysilicon materials are usually composed of lots of grain boundary states. These states are accurately taken care of if a continuous defect state within the band gap of the material is considered. The continuous density of states (DOS) is composed of four types of distribution. Among them two tail bands contain donor-like and acceptor-like states. There are also two deep level bands (Gaussian distribution) for acceptor-like and donor-like grain boundary trap states.

4.3.1 Effect of Tail Distributions

Fig. 4.4 shows the p-type polysilicon NWs subthreshold characteristics at different values of acceptor-like tail state distribution. During the simulation, other parameters remain constant such as N_{GA}=2.5×10^{16} cm^{-3}; N_{TD}=2×10^{17} cm^{-3}eV^{-1}; N_{GD} =2.5×10^{16} cm^{-3}. The donor-like poly-oxide and poly-nitride interface states are kept constant at 1×10^{11} cm^{-2} with two discrete energy levels at E=0.19 eV and E=0.39 eV. The N_{TA} was varied from 5×10^{12} cm^{-3}eV^{-1} to 5×10^{20} cm^{-3}eV^{-1} and it is seen that N_{TA} does not affect the either subthreshold slope or the drive current of the NW. Only a trivial change of leakage current is noticed.

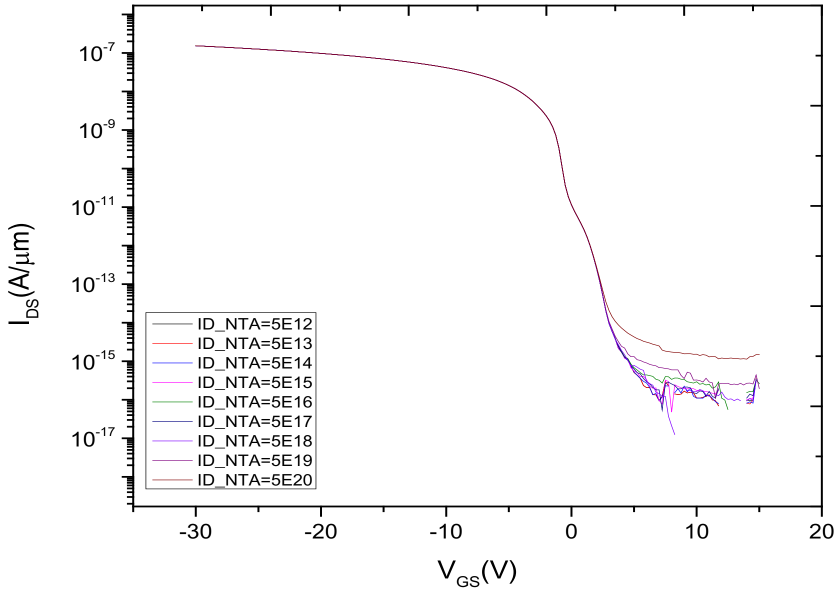

Figure 4.4: Effect of acceptor-like tail distributions.

It can be seen that donor like tail states has effect on both subthreshold slope and drive current. Subthreshold slope increases from 0.72 V/decade to 0.94 V/decade for the increase of N_{TD} from 2×10^{12} cm^{-3}eV^{-1} to 2×10^{20} cm^{-3}eV^{-1} but it does not have effect on leakage current. In addition, drive current also decreases from 1.54×10^{-7} A/µm to 1.64×10^{-8} A/µm for the increase of N_{TD} from 2×10^{12} cm^{-3}eV^{-1} to 2×10^{20} cm^{-3}eV^{-1}.

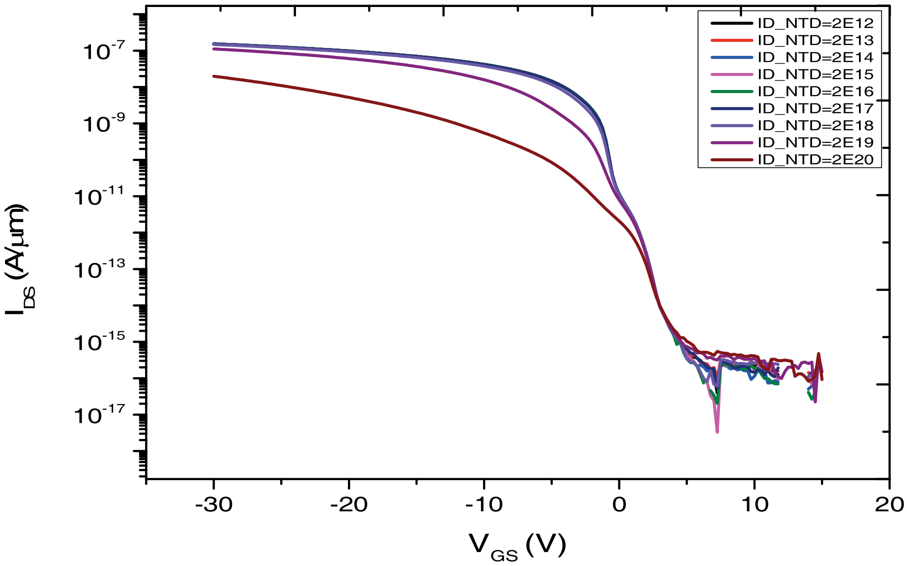

Fig. 4.5 shows the subthreshold slope characteristics of the p-type polysilicon NWs for the donor-like tail distribution. During this simulation, other parameters value remain constant such as N_{TA} =5×10^{17} cm^{-3}eV^{-1}; N_{GA} =2.5×10^{16} cm^{-3}; N_{GD} =2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states are kept constant at 1×10^{11} cm^{-2} with two discrete energy levels at E=0.19 eV and E=0.39 eV.

4.3.2 Effect of Gaussian Distributions

To understand the Gaussian like defect distribution effect, Fig. 4.6 shows the p-type polysilicon NWs subthreshold characteristics at different values of acceptor-like Gaussian state distribution. The density of acceptor-like Gaussian states (N_{GA}) was varied from 2.5×10^{12} cm^{-3}

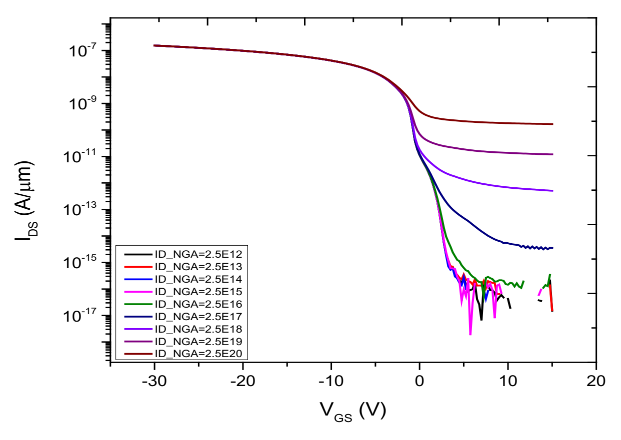

Figure 4.6: Effect of acceptor-like Gaussian distributions (N_{GA}).

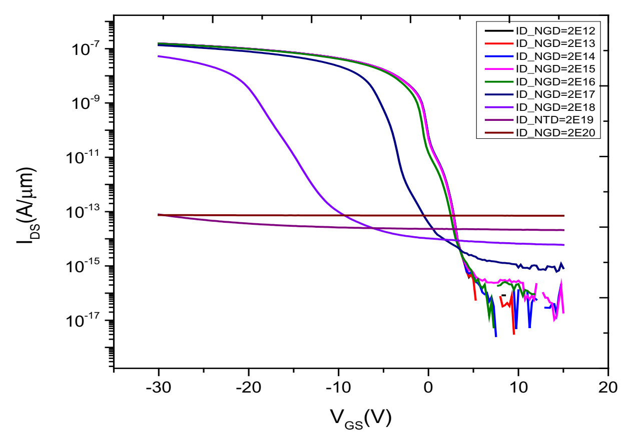

Figure 4.7: Effect of donor-like Gaussian distributions (N_{GD}).

to 2.5×10^{20} cm^{-3} while keeping other parameters constant such as N_{TA} =5×10^{17} cm^{-3}eV^{-1}; N_{TD} =2×10^{17} cm^{-3}eV^{-1}; N_{GD} =2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states were donor-like with the density of 1×10^{11} cm^{-2} which comprised of two discrete energy levels at E=0.19 eV and E=0.39 eV.

It is observed that the variation of N_{GA} affects only the leakage current. Because of the increase of N_{GA} from 2.5×10^{12} cm^{-3} to 2.5×10^{20} cm^{-3}, the leakage current increases from 1.51×10^{-17}A/μm to 5.08×10^{-13} A/μm. It does not have any effect on the subthreshold slope and the drive current.

Fig. 4.7 shows the p-type polysilicon NWs subthreshold characteristics at different values of donor-like Gaussian state distribution. The density of donor-like Gaussian states (N_{GD}) was varied from 2.5×10^{12} cm^{-3} to 2.5×10^{20} cm^{-3}. During this simulation, the other parameters were kept constant with values of N_{TA} =5×10^{17} cm^{-3}eV^{-1}; N_{TD} =2×10^{17} cm^{-3}eV^{-1}; = N_{GA} 2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states of donor-like with the density of 1×10^{11} cm^{-2} which comprised of two discrete energy levels at E=0.19 eV and E=0.39 eV.

From the Fig. 4.7, it can be seen that Gaussian like deep states has significant effects on both subthreshold slope and drive current. Subthreshold slope increases from 0.65 V/decade to 28.97 V/decade for the increase of N_{GD} from 2×10^{12} cm^{-3} to 2×10^{18} cm^{-3} but it does not affect the leakage current. In addition, drive current decreases from 1.56×10^{-7} A/μm to 5.27×10^{-8} A/μm for the increase of N_{GD} from 2×10^{12} cm^{-3} to 2×10^{18} cm^{-3}. From the Fig 4.7 it is also observed that for the value of N_{GD} from 2×10^{19} cm^{-3} to 2×10^{20} cm^{-3} NW does not at all work as transistor and the drive current remain constant around 7.8×10^{-14} A/μm.

The results of Fig. 5.4 to Fig. 5.7 show that the Gaussian like donor state and acceptor state distribution in p-type polysilicon NWs has more effect on the electrical characteristics than of the p-type polysilicon NWs tail like donor state and acceptor state distribution.

4.4 Calibration with Fabricated Polysilicon Nanowire and Extraction of Defect State Distribution

Fig. 4.2 to Fig. 4.7 shows some significant effects of different types of defect states on the p-type polysilicon nanowire. Acceptor like interface trap states are found to affect the leakage current of the nanowire whereas donor like interface traps are found to affect both sub-threshold slope and drive current of nanowire.

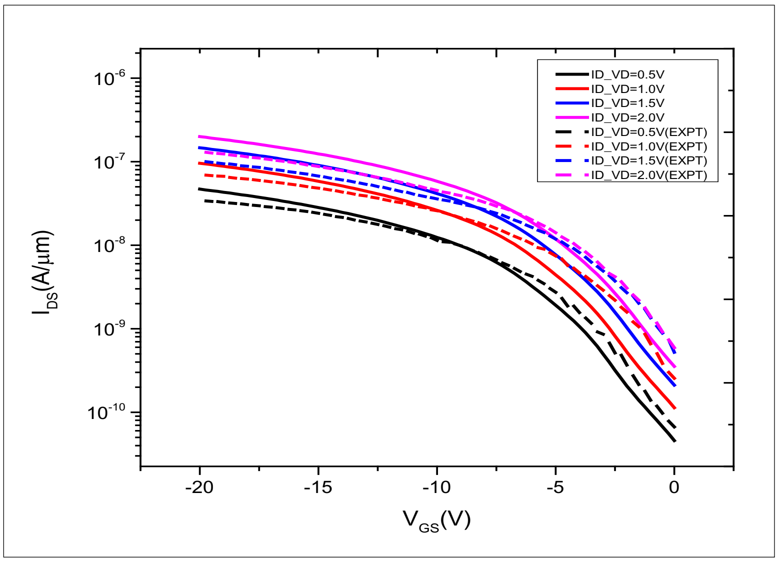

Figure 4.8: Calibration of experimental I_{DS}-$V_{GS}$with simulation.

Defects inside polysilicon also exhibited some important trends. Acceptors like tail states have no effect on the nanowire electrical characteristics whereas acceptor like Gaussian states significantly affects leakage current. However, donor like defects both in tail like and deep level Gaussian like distribution affect nanowire subthreshold characteristics and drive current. However, the effects of donor like Gaussian states are more prominent than tail like states. The aforementioned effects of different types of defects on p-type polysilicon nanowires are used to calibrate nanowires fabricated by deposition and etch as reported in [10]. Throughout our simulation we have created exactly same dimension of polysilicon nanowire and substrate structure like [10]. As fabrication of nanowires were done in class 10 environment, it is well known that interface trap density will be around 10^{11} cm^{-2}. In addition, [10] reports that nanowires were depleted due to surface states and hence, it is reasonably expected that interface traps would be donor like for p-type polysilicon nanowires. As a result in our simulation we have used donor like interface traps. For grain boundary traps, acceptor like states are varied to match leakage current level where as donor like states are varied to match sub-threshold and drive characteristics.

Fig. 4.8 compares simulated transfer characteristics of p-type polysilicon nanowires with experimental results for different drain voltage (V_D=0.5V, 1V, 1.5V and 2V) with the body doping of 6×10^{16} cm^{-3} which is similar to the experimental results [10].

It can be seen that quite a good agreement has been achieved. The drive current of the simulated polysilicon nanowire is quite similar with the fabricated polysilicon nanowire and subthreshold characteristics are also comparable with the experimental results. Such a calibration has allowed us to extract polysilicon nanowires defect states which was fabricated by deposition and etch technology.

The extracted parameters are summarized below

Table 4.1: Trap states distribution parameters and device parameters used for simulation

Device Parameter	Symbol (Units)	Value
Channel Length	$L(\mu m)$	10
Channel Width	$W(\mu m)$	0.1
Oxide Thickness	$t_{ox}(nm)$	10
Polysilicon Thickness	$t_{si}(nm)$	100
Nitride Thickness	$t_{nitride}(nm)$	500
Silicon Thickness (n-type)	$t_{silicon}(nm)$	500
Back Gate Thickness	$t_{backgate}(nm)$	10
Source and Drain Dopant Density	$p^{+}(cm^{-3})$	1×10^{20}
Polysilicon Doping Density	$p^{+}(cm^{-3})$	6×10^{16}
Silicon Substrate Doping Density	$n^{+}(cm^{-3})$	1×10^{16}
Capture Cross Section of Electrons in Acceptor –like States	$\sigma_{ae}(cm^{2})$	1×10^{-16}
Capture Cross Section of Holes in Acceptor –like States	$\sigma_{ah}(cm^{2})$	1×10^{-14}
Capture Cross Section of Electrons in Donor –like States	$\sigma_{de}(cm^{2})$	1×10^{-14}
Capture Cross Section of Holes in Donor –like States	$\sigma_{dh}(cm^{2})$	1×10^{-16}
Density of Acceptor-like Tail States	$N_{TA}(cm^{-3}eV^{-1})$	2×10^{19}
Density of Donor-like Tail States	$N_{TD}(cm^{-3}eV^{-1})$	1.12×10^{18}
Density of Acceptor-like Gaussian States	$N_{GA}(cm^{-3})$	1×10^{18}
Density of Donor-like Gaussian States	$N_{GD}(cm^{-3})$	1×10^{17}
Decay Energy for Acceptor-like Tail States	$W_{TA}(eV)$	0.05
Decay Energy for Donor-like Tail States	$W_{TD}(eV)$	0.05
Decay Energy for Acceptor-like Gaussian States	$W_{GA}(eV)$	0.1
Decay Energy for Donor-like Gaussian States	$W_{GD}(eV)$	0.1
Energy of Gaussian for Acceptor-like States	$E_{GA}(eV)$	0.51
Energy of Gaussian for Acceptor-like States	$E_{GD}(eV)$	0.51

Capture Cross Section of the Trap for Electrons at Interface	$\sigma_n(cm^2)$	1×10^{-14}
Capture Cross Section of the Trap for Holes at Interface	$\sigma_p(cm^2)$	1×10^{-16}
Density of Donor-like Interface Trap States	$D_{it}(cm^{-2})$	1.18×10^{11}
Degeneracy Factor		1

The Table 4.1 describes all and shows that the result $(I_{DS} - V_{GS})$ matches for all V_{DS} (0.5V, 1V, 1.5V and 2V) and the result $(I_{DS} - V_{DS})$ matches for all V_{GS} (0.0V, -5V, -10V, -15V and -20V).

4.5 Discussion

We have investigated the effect of interface traps and p-type polysilicon grain boundary defects on the electrical characteristics of p-type polysilicon nanowires (NWs). It has been observed that acceptor-like interface trap states affect the leakage current of the NW whereas donor-like interface traps affect both subthreshold slope and drive current of NW. Defects inside polysilicon also exhibited some important trend. Acceptor-like tail states have not affected the NW electrical characteristics whereas acceptor-like Gaussian states have significantly affected the leakage current. However, donor-like defects both in tail like and deep level Gaussian like distribution have affected NW subthreshold characteristics and drive current. These physical understandings of different types of defects are used to calibrate p-type polysilicon NW fabricated by deposition and etch technique which allowed us to extract different types of defects. This knowledge is very important to explain the p-type polysilicon NW biosensor behavior that has been recently shown to be the only viable route for mass manufacture of NW biosensors. Once the device platform with polysilicon nanowires are calibrated with the experiment, the polysilicon material is replaced with single crystal silicon material to predict single crystal nanowire behaviour.

CHAPTER 5

5. ASSESSMENT OF SINGLE CRYSTAL SILICON NANOWIRE

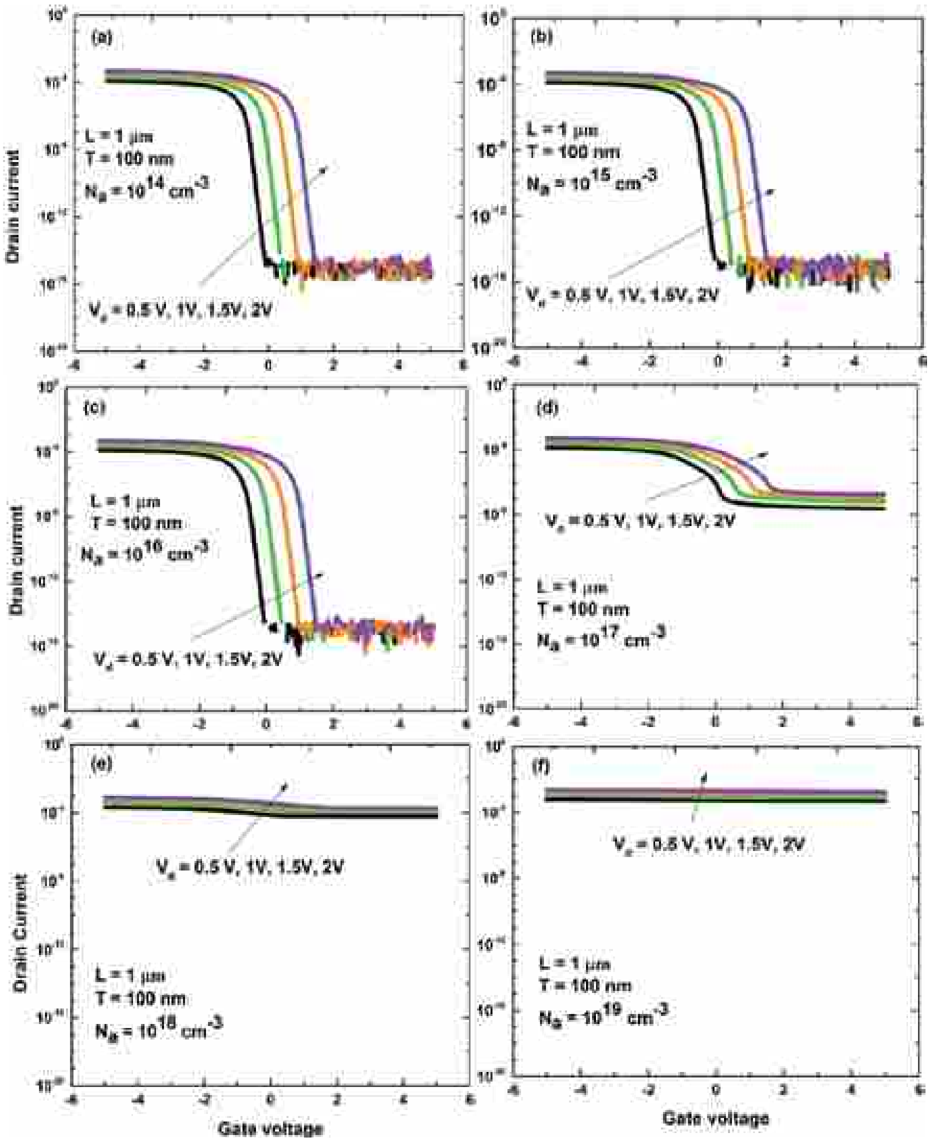

Figure 5.1: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1µm *(Continued to next page)*.

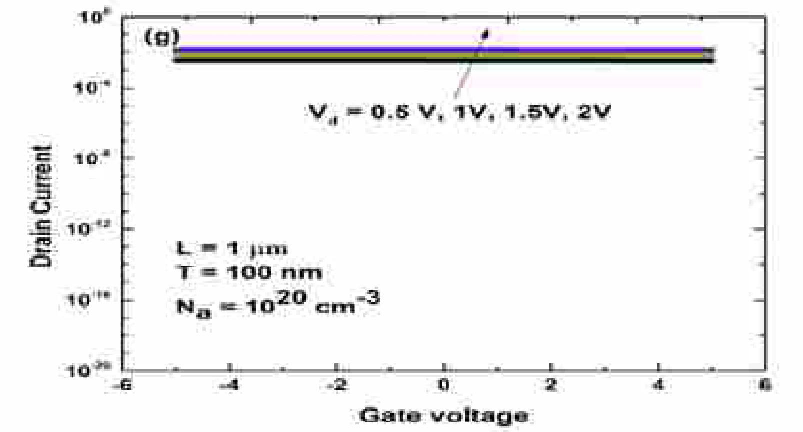

Figure 5.1 ***(continued)*****:Transfer characteristics ($I_D$vsV_G) of accumulation mode Si-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.**

Fig. 5.1 shows the transfer characteristics ($I_D$vsV_G) of accumulation mode SI-NW transistors with a NW thickness of 100nm and for different doping concentrations. For 100nm NW thickness, it can be observed that nanowires exhibit excellent transistor like behavior for doping concentration 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3}(Fig. 5.1 (a), (b) and (c)) with sub- threshold slopes of 66.47 mv/decade, 66.47 mv/decade and 67.92 mv/decade at drain voltage of 0.5 V. At the doping concentration 10^{17}cm^{-3} (Fig.5.1 (d)), the sub threshold slope is 777.33 mv/decade which implies quite abad transistor behavior. At the doping concentration 10^{18} cm^{-3},10^{19} cm^{-3} and 10^{20} cm^{-3} (Fig. 5.1 (e), (f)and (g)), devices exhibit resistor like behavior rather than transistor.

Fig. 5.2 shows the transfer characteristics ($I_D$vs V_G) of accumulation mode Si-NW transistors with a NW thickness of 5nm and for different doping concentrations. For 5nm NW thickness, it is found that the nanowires exhibit quite a good transistor behavior for doping concentration 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3}(Fig. 5.2 (a), (b) and (c)) with subthreshold slopes of 61.15 mv/decade, 61.15 mv/decade and 61.15 mv/decadewhich is similar to that of the 100nm NW thickness. However, unlike 100nm thickness, Si-NW transistors with 5nm thickness also show excellent transistor behavior for doping concentrations of 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}with subthreshold slopes of 61.15 mv/decade, 61.92 mv/decade and 65.6 mv/decade (Fig. 5.2 (d), (e) and (f)). However, for 10^{20} cm^{-3} doping concentration, 5nm Si NW transistor shows degraded transistor behavior with sub-threshold slope of 7552.3 mv/decade, which is preferable to accept as resistor like characteristics.

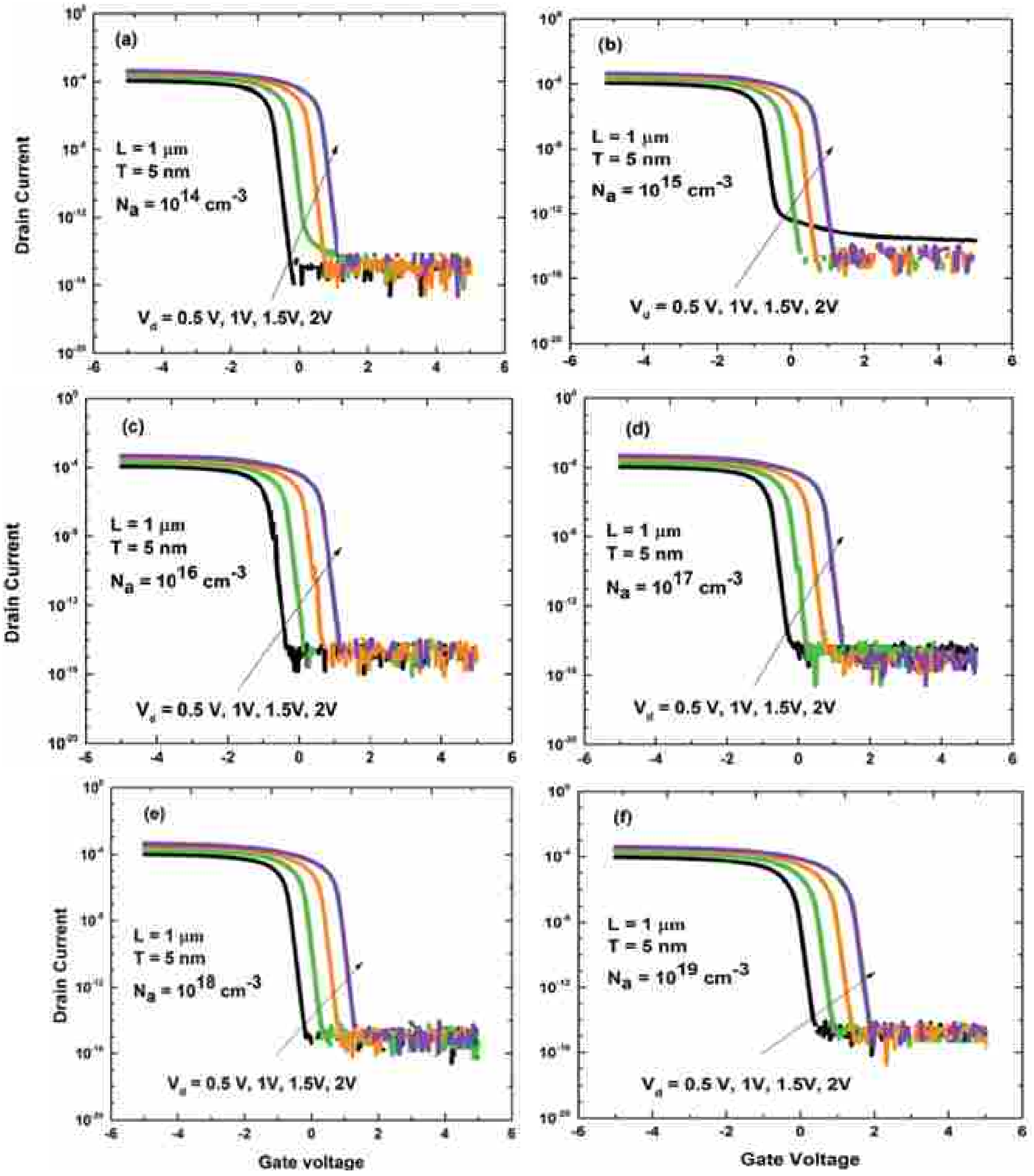

Figure 5.2: Transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1µm. *(Continued to next page)*

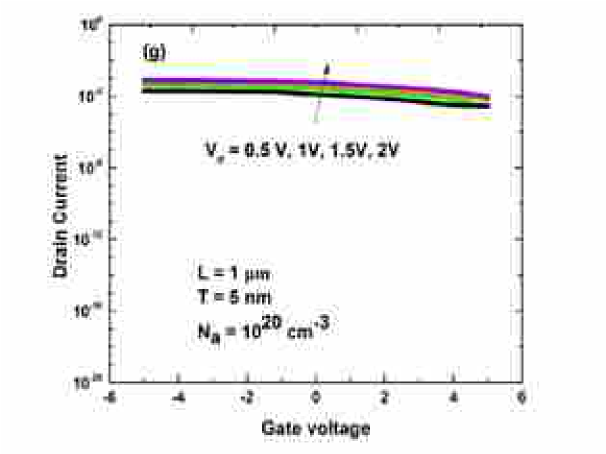

Figure 5.2 *(continued):* Transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

To characterize the NW behavior in more details, I_D vs$V_d$curves are generated for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. Fig. 5.3 shows the output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with a NW thickness of 100nm and for different doping concentrations. It is seen that for doping concentration of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} (Fig. 5.3 (a), (b) & (c)) the drain currents show significant change with gate voltage, which implies that in these doping concentrations nanowires behave like transistors. In the doping concentration of 10^{17} cm^{-3}(Fig. 5.3 (d)), though a noticeable change in the drain current with gate voltage is found, actually at this doping concentration a weak transistor like behavior exists with a sub threshold slope of 777.33 mv/ decade (Fig. 4.2 (d)) which is not readily visible in output characteristics of MOSFETs. In doping concentration 10^{18} cm^{-3}(Fig. 5.3 (e)) nanowire's drain current modulation with gate voltage is reduced, whereas in doping concentration 10^{19} cm^{-3} and 10^{20} cm^{-3}(Fig. 5.3 (f) & (g) no gate effect on the drain current is observed. These results indicate that 100 nm Si NW transistors show good transistor behavior for doping concentration of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3}. When doping concentration is increased from 10^{17} cm^{-3} to 10^{20} cm^{-3} Si NW gradually coverts from weak transistor to resistors due to the gradual loss of gate control. However, with the increase of the doping concentration from 10^{14} cm^{-3} to 10^{20} cm^{-3}, the drain current of 100 nm Si NW's are increased for any particular V_D and V_G.

Fig. 5.4 shows the output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with a NW thickness of 5 nm and for different doping concentrations. It is observed that the drain currents show significant change with gate voltage for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} (Fig. 5.4 (a), (b) and (c))which implies that in these doping concentrations, nanowires exhibit transistor action which is the similar behavior that is observed for 100nm NW thickness at these doping concentrations. However, unlike 100 nm Si NW thickness, 5 nm NWs exhibit excellent transistor behavior for doping concentrations of 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. However, at doping concentration of 10^{20} cm^{-3}5nm,Si NWs shows degraded transistor behavior which is similar to the observed in the output characteristics 100 nm Si NWs at the doping concentration of 10^{18} cm^{-3}(Fig. 4.3(e)).

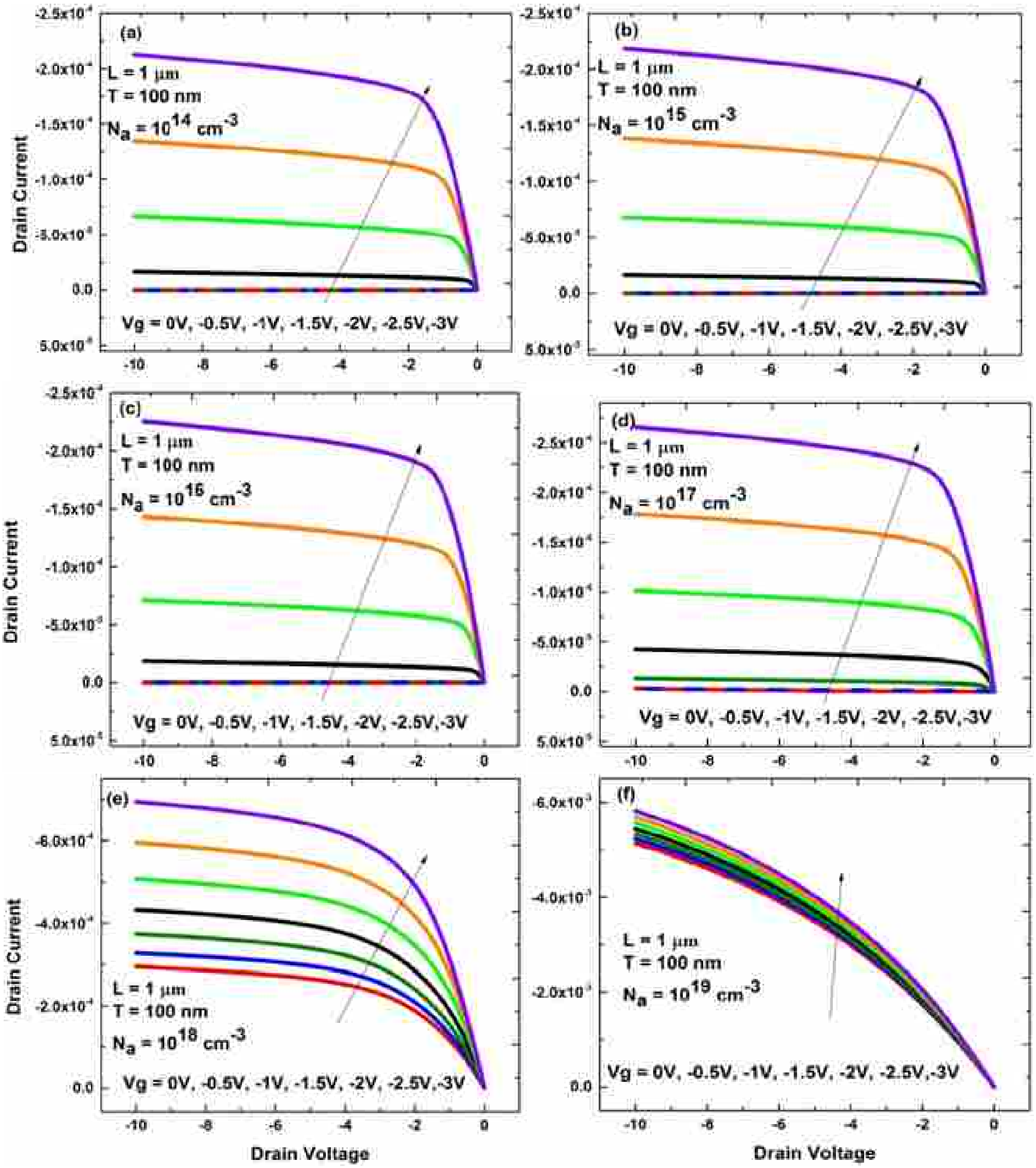

Figure 5.3:Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1µm. ***(Continued to next page)*.**

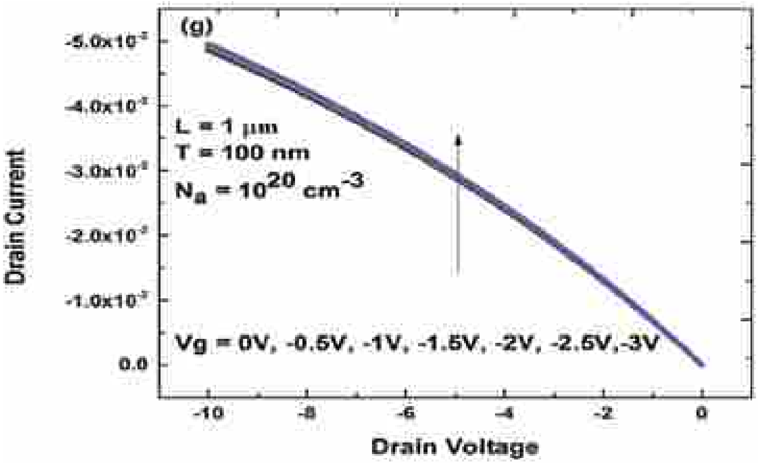

Fig. 5.3 ***(Continued)*****: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.**

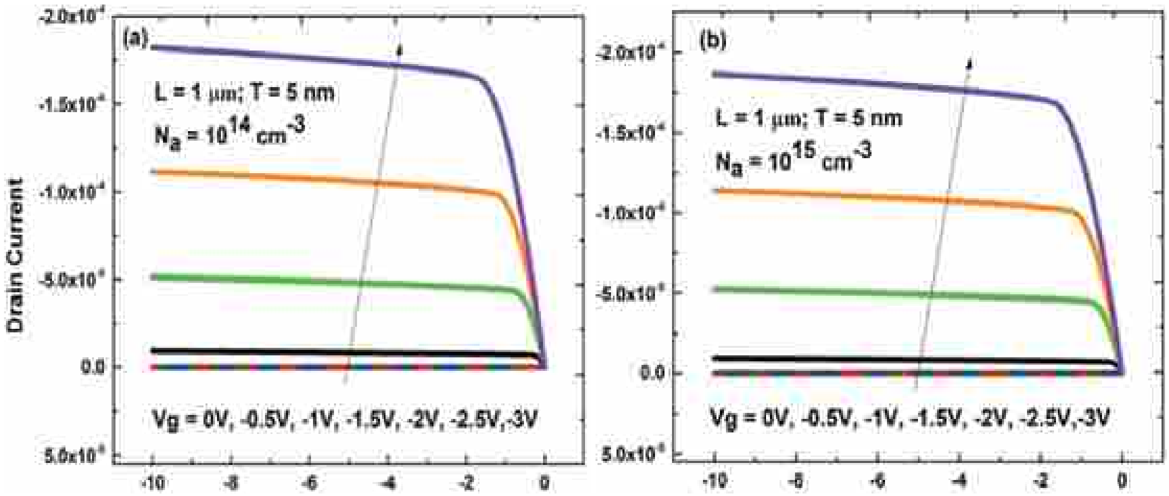

Figure 5.4: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. ***(Continued to next page).***

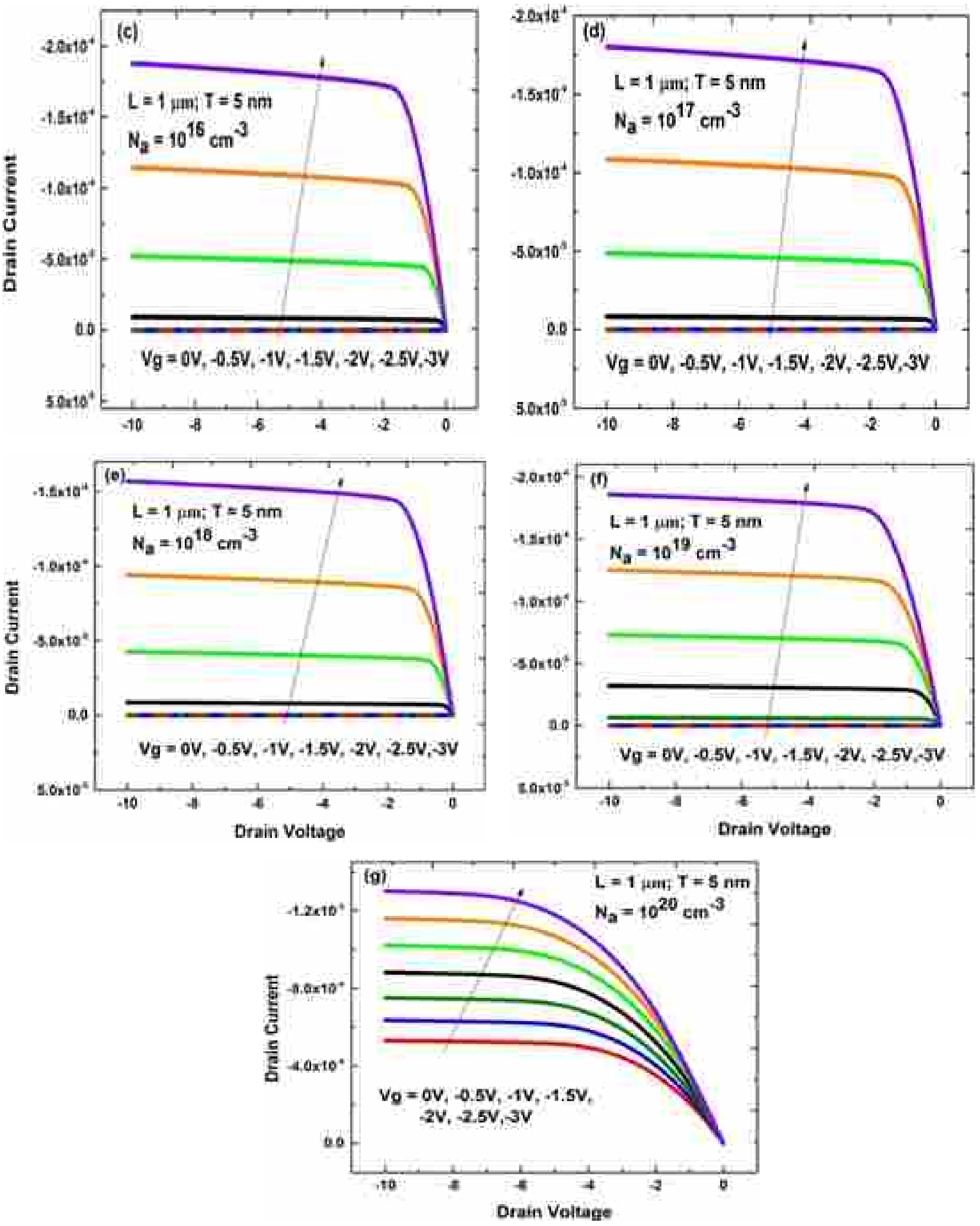

Figure 5.4 ***(Continued):*** **Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.**

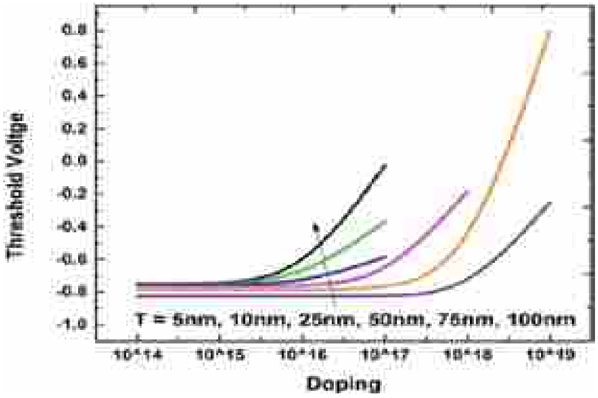

Figure 5.5: Threshold voltage verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage 0.5v.NWs have channel length of 1µm.

Fig. 5.5 shows threshold voltage as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage of 0.5v. For 100nm NW thickness, threshold voltages remain constant around -0.75v for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3} and 10^{16} cm^{-3} while devices exhibit excellent transistor behavior (Fig. 5.1). At the doping density of 10^{17} cm^{-3}threshold voltage found to be -0.025 V implying that quite a less amount of accumulation is enough to reach threshold current. This can be attributed to the fact that for 100 nm NW thickness depletion strength is less for the doping density of 10^{17} cm^{-3}and hence, some conduction could occur within the body of the nanowire which also explains the bad transistor behavior of 100 nm NW at this doping (Fig. 5.2). Above 10^{17} cm^{-3}doping density no threshold voltage could be extracted for 100 nm NWs as devices behave as resistor rather than transistor (Fig. 5.1).For 5nm NW thickness, threshold voltages are around -0.8 V for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3} and 10^{18} cm^{-3} and devices again exhibit excellent transistor behavior (Fig. 5.2).Although for doping density of 10^{19} cm^{-3}5 nm nanowires exhibiting a less negative threshold voltage of -0.25v and hence, the device required less accumulation to reach threshold current, it is still exhibiting good transistor behavior due to high volume constriction of 5 nm thick NW. In general Fig. 5.5 also shows that with decreasing NW thicknesses threshold voltages of NWs at different doping density is becoming more negative which can be easily understandable as thin NWs have more constricted volume and hence, strong effect of depletion thereby requiring strong negative potential to reach threshold current.

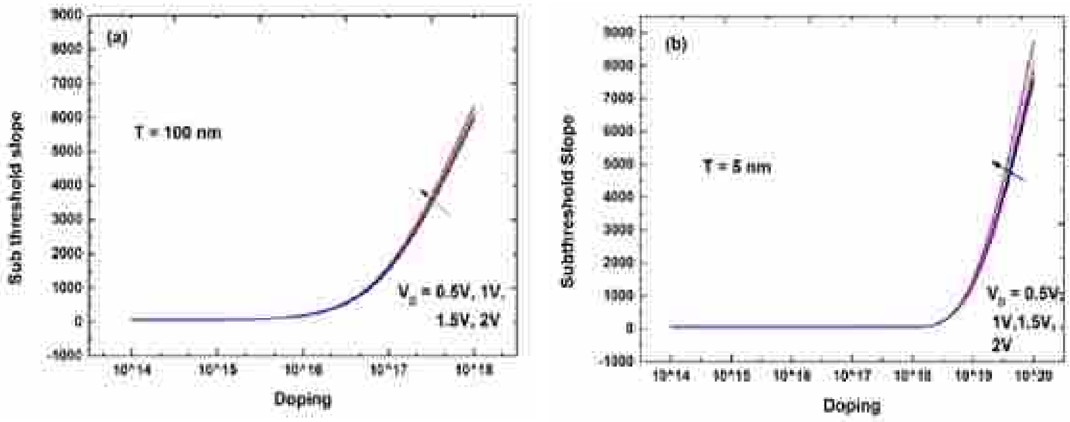

Figure 5.6: Sub threshold slope verses Doping for NW thicknesses a) 100nm and b) 5nm.NWs have channel length of 1µm.

Fig. 5.6 shows sub threshold slopes as a function of doping at different drain voltagesi.e, 0.5 V, 1 V, 1.5 V and 2 V for NW thicknesses of (a) 100nm and (b) 5nm. For 100nm NW thickness in Fig. 5.6 (a),sub-threshold slope is found to be around 67 mV/decade for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3}and 10^{16} cm^{-3}for drain voltages of 0.5 V, 1 V, 1.5 V and 2 V. At these doping densities 100 nm Si NW exhibits excellent transistor behavior (Fig. 5.1) and the interesting phenomenon is that no degradation of sub-threshold slope could be observed with increasing drain bias in accumulation mode Si NW transistors like conventional inversion mode MOSFETs. However, above these doping densities, 100 nm accumulation mode Si NW transistors gradually exhibit weak transistors to resistor like behavior and slight degradation in the sub-threshold slopes can be observed with increasing drain bias. For 5nm NW thickness in Fig. 5.6 (b), sub-threshold slope is found to be around 61 mV/decade for doping concentrations of 10^{14} cm^{-3} to 10^{19} cm^{-3}for all drain voltages of 0.5 V, 1 V, 1.5 V and 2 V. Again at these doping densities, while 5 nm Si NW exhibit excellent transistorbehavior (Fig. 5.2), no degradation of sub-threshold slope could be observed with increasing drain bias in accumulation mode Si NW transistors. Similar behavior is observed in the sub-threshold characteristics for other NW thicknesses.

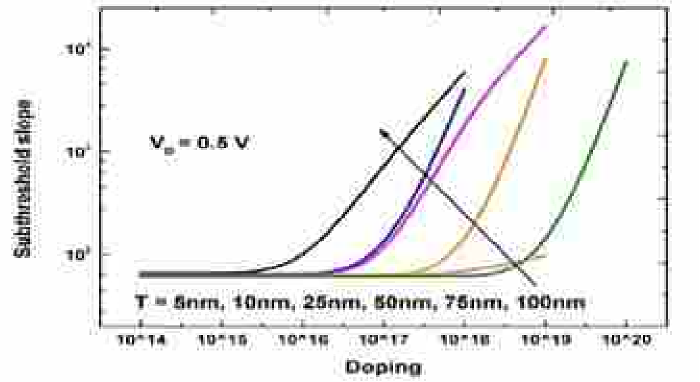

Figure 5.7: Sub threshold slope verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage 0.5 v. NWs have channel length of 1µm.

Fig. 5.7 shows sub-threshold slope as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage of 0.5v. For 100nm NW thickness, sub-threshold slopesare around 67 mv/decade for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3}, and 10^{16} cm^{-3}. As discussed before, with increasing doping densities from 10^{17} cm^{-3}to 10^{18} cm^{-3}sub-threshold slopeis gradually degraded in 100 nmaccumulation mode Si NW transistors. For 5nm NW thickness, again sub-threshold slopes remain constant around 61 mv/decade for doping concentrations of 10^{14} cm^{-3} to 10^{19} cm^{-3} and at the doping density of 10^{20} cm^{-3} 5 nm Si NW accumulation mode transistor shows hardly any transistor action with a sub-threshold slope around 75552 mV/decade. However, it is worth noting that with the decrease of Si NW thicknesses sub-threshold slopes are gradually becoming more ideal for the doping densities while NWs are exhibiting transistor like behavior.

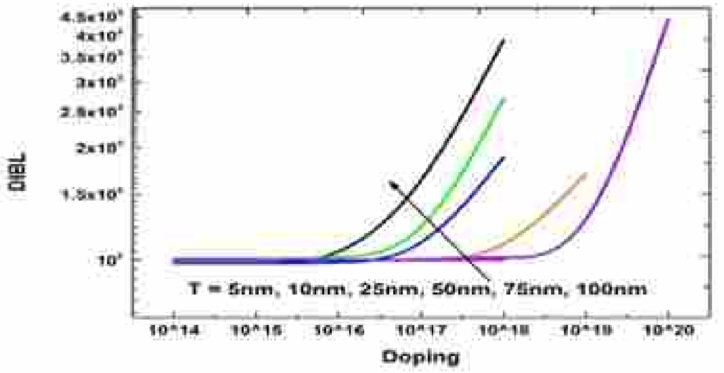

Figure 5.8: DIBL verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm.

Fig. 5.8 shows DIBL as a function of doping concentrations for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm. The DIBL behavior of accumulation mode NW transistors at different NW thicknesses and doping densities exhibit exactly similar behavior of threshold voltages and sub-threshold slopes as observed in Fig. 5.5 and Fig. 5.7 respectively. For example, at 100nm NW thickness, DIBL value remain constant around 982 mv/vfor doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3} whereas this parameter gets degraded to values 1500 mv/v and 3900 mv/v for doping concentrations of 10^{17} cm^{-3} and 10^{18} cm^{-3} when NW shows weak transistor or almost resistor like behavior. For 5nm NW thickness, DIBL values are almost similar to that of the 100 nm NW thickness with a value around 1000 mv/v for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. Again at doping concentration of 10^{20} cm^{-3}, 5 nm Si NW exhibit degraded value of 4440mv/v. It is worth noting that while accumulation mode Si NW transistors exhibit plausible transistor action, DIBL does not significantly change with NW thicknesses for the 1µm channel length NWs.

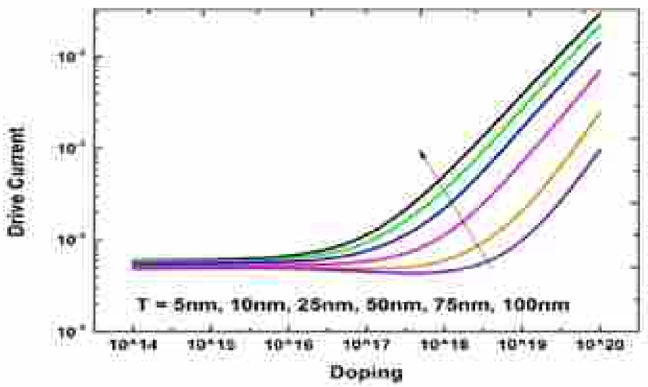

Figure 5.9: Drive Current verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm.NWs have channel length of 1µm.

Fig. 5.9 shows drive current as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm. In general drive current accumulation mode, NW transistors decreases with the decrease of NW thicknesses at all doping densities which is a quite expected phenomenon due to the constriction of conduction volume. However, it is worth noting that the drive current reduction is quite significant in the doping concentrations when NWs either exhibit poor transistor action and/or resistor like behavior.

DISCUSSION

The results show that accumulation mode transistor behavior is strongly dependent on doping and NW thicknesses. For 100nm NW thickness, it is observed that nanowires exhibit excellent transistor like behaviorfor doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}. An increase in the doping concentration into 10^{17} cm^{-3}orabove gradually converts 100 nm Si NWs into weak transistor or simple resistors. For 5nm NW thickness, excellent transistor action is observed for a broad range of doping concentrations such as, 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. Again at doping concentration of 10^{20} cm^{-3} 5 nm Si NW exhibit resistor like behavior. These results indicate that with the decrease of NW thicknesses, Si NW works as accumulation mode transistor at significantly high level of doping concentrations.

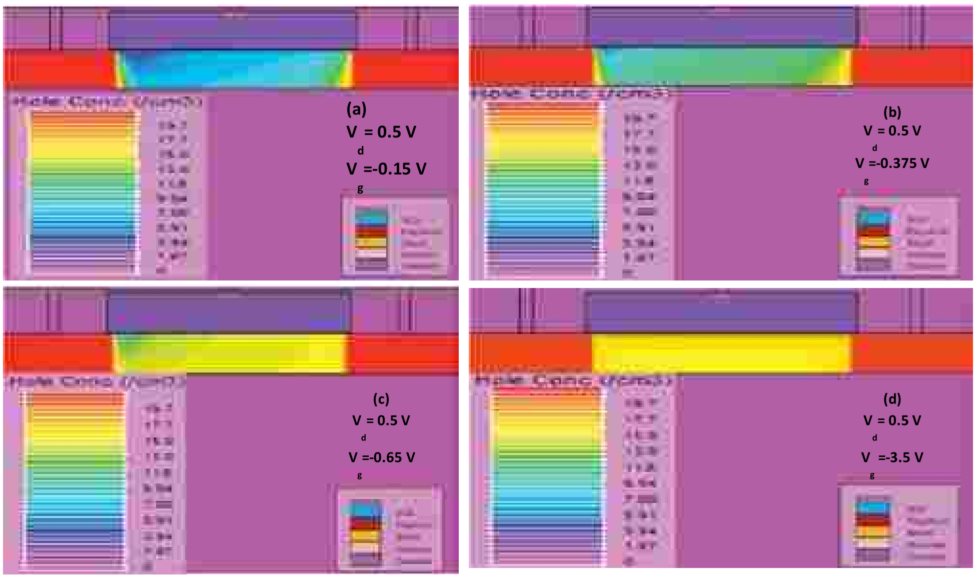

Figure 5.10: Hole concentration contour plots of 100 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V; a). At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V, b) at the middle part of the linear section of sub-threshold plot with a V_g = -0.375V, c) at the top part of the linear section of sub-threshold plot with a V_g = -0.375V (just before saturation) and d) at saturation with a V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting transistor like behavior.

To explain this phenomenon, Fig. 5.10 shows hole concentration contour plots of the 100 nm Si NW at different points of sub-threshold region for a doping concentration of 10^{14} cm^{-3} while 100 nm NW is behaving as an excellent transistors. At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V (Fig. 5.10(a)), it can be seen that hole concentration varies from around10^3 cm^{-3} to 10^6 cm^{-3} at different regions of the channel. For a doping density of 10^{14} cm^{-3}, such amount of free holes is actually representing full depletion of the channel. At the middle part of the linear section of sub-threshold plot with a V_g = -0.375V (Fig. 5.10(b)), hole concentrations are around 10^{12} cm^{-3} to 10^{13} cm^{-3} at the most of the sections of thechannel. Such an amount of carrier concentrations represents mild accumulation. However, it is worth noting that accumulation is not uniform in the whole volume of the NW. Just before saturation with a V_g = -0.65V(Fig. 5.10(c)) increased accumulation can be seen with hole concentration varying from around 10^{14} cm^{-3} to 10^{16} cm^{-3} again with a non-uniform distribution along the volume of the NW channel. At saturation with a V_g = -3.5V (Fig. 5.10(d)), it can be seen that hole concentration varies from around 10^{16} cm^{-3} to 10^{17} cm^{-3} in the most of the region of the NW channel with better uniformity thanFig. 5.10(a), (b) & (c). However, a thin layer with a hole concentration of around 10^{20} cm^{-3}can also be seen at the top region of the NW channel which is close to gate. This result indicates that with the increase of the negative gate bias, 100 nm NW with a doping density 10^{14} cm^{-3} gradually converts from depletion to partial accumulation to full accumulation of the channel volume. The transition from depletion to partial accumulation of the NW volume results in the linear section of the sub-threshold plot whereas the full accumulation of the volume results in the saturation of the drain current and hence, 100 nm Si NW with a doping concentration of 10^{14} cm^{-3} shows an excellent transistor behavior.

Fig. 5.11shows hole concentration contour plots of 100 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V. 100 nm thick Si NWs are exhibiting resistor like behavior at this doping concentration. At the V_g = -0.15V (Fig. 5.11(a)), it can be observed that whole volume of the NW has a hole concentration of around 10^{19} cm^{-3} except for a tiny depletion region near the gate with a hole concentration around 10^{15} cm^{-3}. Similar behavior can be observed for V_g = -0.375V (Fig. 5.11(b)), with a hole concentration of around10^{19} cm^{-3} in the whole volume ofthe 100 nm NW. However, the tiny depletion region near the gate appears to be reduced at this gate voltage. For V_g = -0.65V and V_g = -3.5V (Fig. 5.11(c) & (d)), no depletion region can be seen in the 100 nm NW but the whole volume remains conductive with a hole concentration around10^{19} cm^{-3}. This result indicates that for 100 nm NW thickness with a doping concentration of 10^{19} cm^{-3}, there is no effect of gate voltages and quite a significant conduction path exists approximately through the whole volume of the NW at all gate voltages. As a result, 100 nm thick NW at this doping density shows resistor like behavior.

To explain the transistor like behavior of 5 nm thick NW at the doping density of 10^{14} cm^{-3}, Fig. 5.12shows hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V. The behavior of 5 nm thick Si NW at this doping concentration (Fig. 5.3) is similar to the 100 nm thick Si NW at the doping density of 10^{14} cm^{-3}(Fig. 5.1). The hole concentration in the volume of the NW is found to be around 10^{7} cm^{-3} to10^{9} cm^{-3}, 10^{11} cm^{-3} to10^{13} cm^{-3}, 10^{14} cm^{-3} to10^{17} cm^{-3} and 10^{18} cm^{-3} to10^{20} cm^{-3} at gate voltages of -0.15V, -0.375V, = -0.65V and -3.5V respectively. This result indicates that significant gate modulation exists for 5 nm NW with a doping density 10^{14} cm^{-3} and with the increase of negative gate bias,NW volume gradually converts from depletion to partial accumulation to full accumulationexplaining its transistor like behavior.

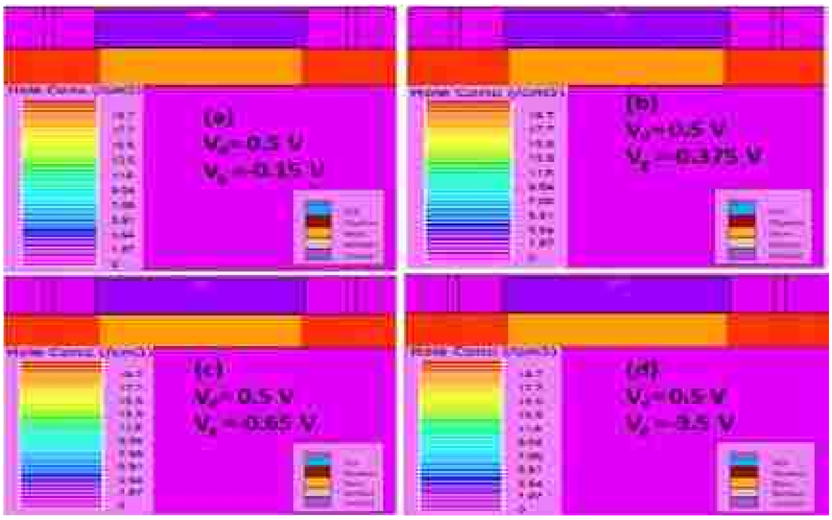

Figure 5.11: Hole concentration contour plots of 100 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V; a) for V_g = -0.15V, b) for V_g = -0.375V, c) for V_g = -0.375V and d) for V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting resistor like behavior.

Finally we explain transistor like behavior of 5 nm thick NW at the doping density of 10^{19} cm^{-3}. Atthis doping density 100 nm thick Si NW showed resistor like behavior rather than transistor action. Fig. 5.13 shows hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V. Unlike 100 nm NWs, where gate effect was observed in a tiny volume near the gate at this doping density (Fig. 5.11), 5 nm thick Si NW experienced a significant gate modulation all through its volume. The hole concentration in the volume of the 5 nm thick, NW (Fig. 5.13) is found to be around 10^{12} cm^{-3} to10^{15} cm^{-3}(with most of the volume at 10^{15} cm^{-3}), 10^{16} cm^{-3} to10^{17} cm^{-3}(with most of the volume at 10^{16} cm^{-3}), 10^{16} cm^{-3} to10^{17} cm^{-3}(with most of the volume at 10^{17} cm^{-3}) and 10^{19} cm^{-3} to10^{20} cm^{-3}(with most of the volume at 10^{19} cm^{-3}and a flat region near the gate with 10^{20} cm^{-3}) at gate voltages of -0.15V, -0.375V, = -0.65V and -3.5V respectively. At the doping density of 10^{19} cm^{-3}, a tiny region is expected to be affected by gate. Significant volume constriction in the 5 nm thick NW appears to be sufficient for such modulation all through its volume and with the increase of negative gate bias,5 nm thick NW volume was able to be gradually converted from depletion to partial accumulation to full accumulationthereby explaining its transistor like behavior. Gate voltage modulation on a very small volume at the doping density of 10^{19} cm^{-3}also explains why 100 nm thick Si NW at this doping behaved as a resistor rather than transistor. These investigations (Fig. 5.10 to 5.133) also imply that with the increase of the doping density as the gate, modulated volume gradually decreases. , The whole volume can be affected only when NWs are thin and have constricted volumes and hence, thin NWs are able to exhibit transistor action at high doping density like 10^{19} cm^{-3} which is close to source/drain doping of conventional MOSFET. In contrast, significant conduction path exists beyond the gate modulated volume of thick nanowires at high doping densities and hence, thick nanowires fail to show accumulation mode transistor action at high doping densities.

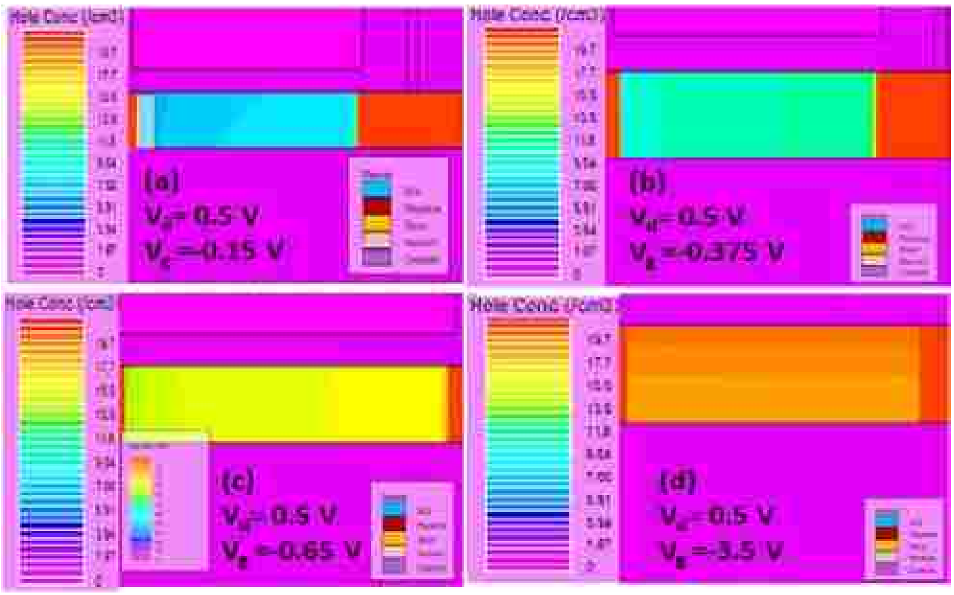

Figure 5.12: Hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V; a) At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V, b) at the middle part of the linear section of sub-threshold plot with a V_g = -0.375V, c) at the top part of the linear section of sub-threshold plot with a V_g = -0.375V (just before saturation) and d) at saturation with a V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting transistor like behavior.

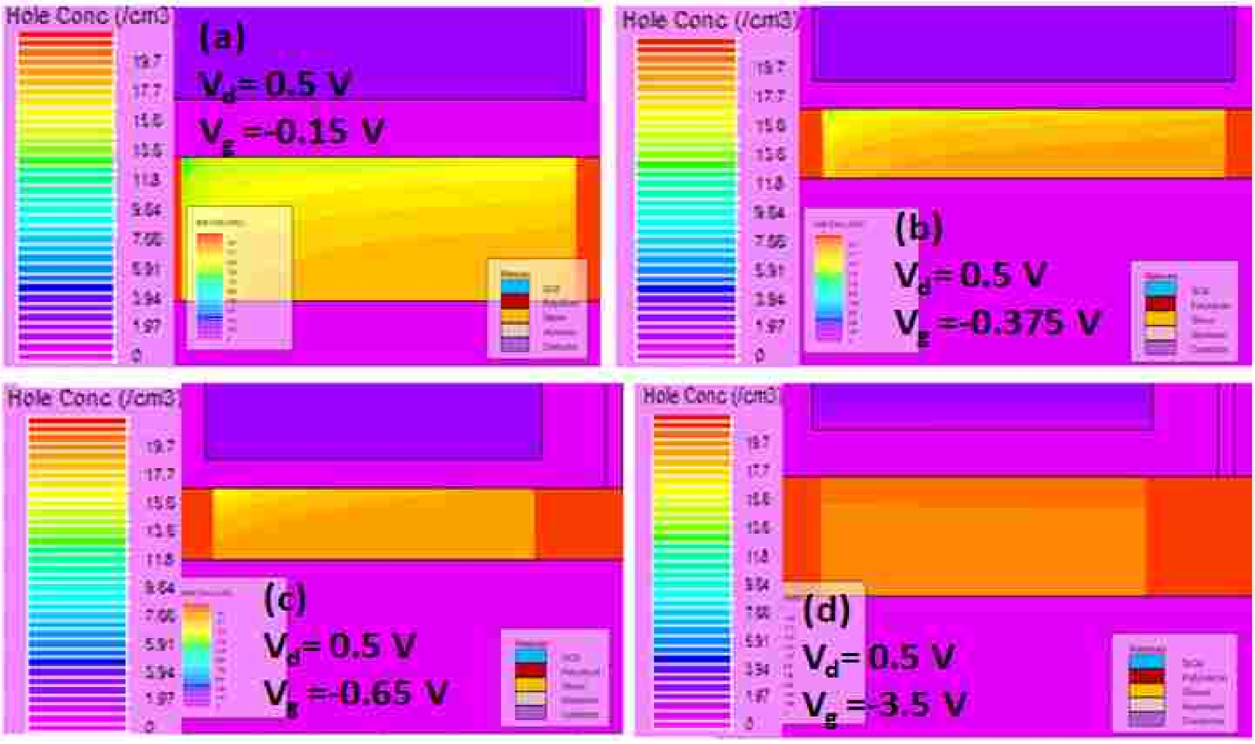

Figure 5.13: Hole concentration contour plots of 5 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V; a) for V_g = -0.15V, b) for V_g = -0.375V, c) for V_g = -0.375V and d) for V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting resistor like behavior.

CHAPTER 6

6. ASSESSMENT OF POLY-CRYSTALLINE SILICON NANOWIRE

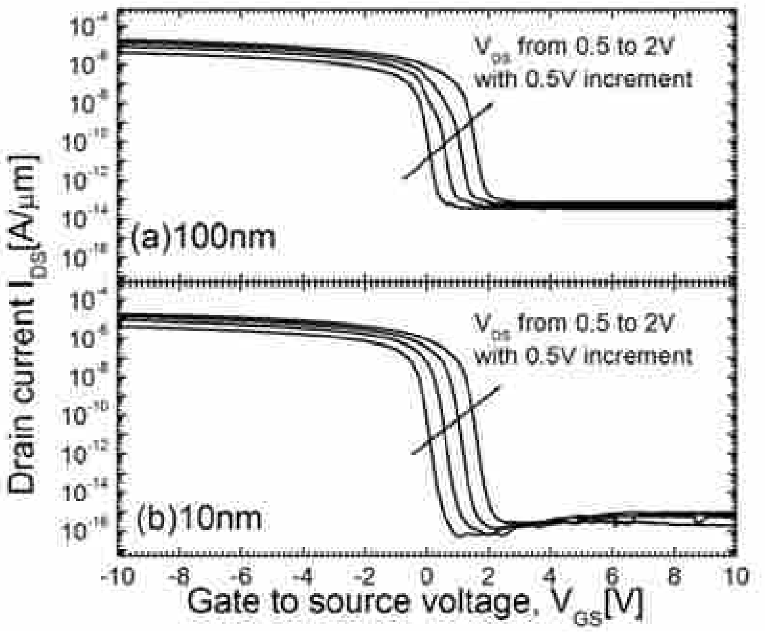

Figure 6.1: Transfer characteristics of p-type polysilicon nanowires with 10^{16}/cm^3 doping concentration at different thicknesses; (a) 100nm and (b) 10nm.

In this chapter we study the effect of nanowire thicknesses and doping concentrations on the electrical characteristics of polycrystalline silicon nanowires to find out the proper combination of nanowire thickness and doping for sensitive operation of polycrystalline silicon nanowire biosensors. For nanowire thicknesses of 100 nm and 75 nm, a plausible sub-threshold slope around 100 mV/dec for a viable biosensor operation can only be achieved if doping concentration is 2×10^{16}/cm^3 or below. For a 50 nm nanowire thickness, a relatively wide doping concentration range can be chosen for biosensor design while maintaining decent sub-threshold characteristics. In this thickness a doping up to 4×10^{17}/cm^3 with a sub-threshold slope around 100 mV/dec can be chosen. The widest range of doping concentrations can be chosen for 25 nm and 10 nm nanowire thicknesses with a maximum doping up to 10^{18}/cm^3 while maintaining a promising sub-threshold slope around 95 mV/dec for a viable biosesnsor design using polycrystalline silicon nanowires. As such this research reveals the possible combinations of nanowire thickness and doping to ensure the sensitive operation of polycrystalline silicon nanowire biosensors.

Figure 6.1 shows transfer characteristics (I_{DS} vs V_{GS}) of p-type Si-NWs for different nanowire thicknesses. The length of the nanowire is 10 μm and the doping density is 10^{16}/cm^3. For the naowire thickness of 100 nm in figure 6.1 (a), the sub-threshold slope is found to be 102.61 mV/decade and the DIBL is found to be around 1030 mV/V. Although the value of sub-threshold slope is much higher than the ideal value of 60 mV/decade, it is still suitable for biosensor operation considering the fact that gate charge modulation can be detected if operating point of the bio-sensor can be set within the linear region of the sub-threshold regime. For the nanowire thickness of 10 nm in figure 6.2(b), the sub-threshold slope and DIBL are found to be 93 mV/decade and 980 mV/V. The sub-threshold characteristic at this thickness is much better than that of the 100 nm thickness and the sub-threshold slope is also close to the ideal value of 60 mV/V. Hence, 10 nm thick 10 μm long nanowire with a doping of $10^{16}/cm^3$ is a promising candidate for biosensor application as setting the operating point within the linear region of sub-threshold region would ensure an excellent response to the gate charge modulation upon immobilization of analytes. These results imply that 100 nm to 10 nm thick polysilicon nanowires can be used as biosensor with a doping density of $10^{16}/cm^3$.

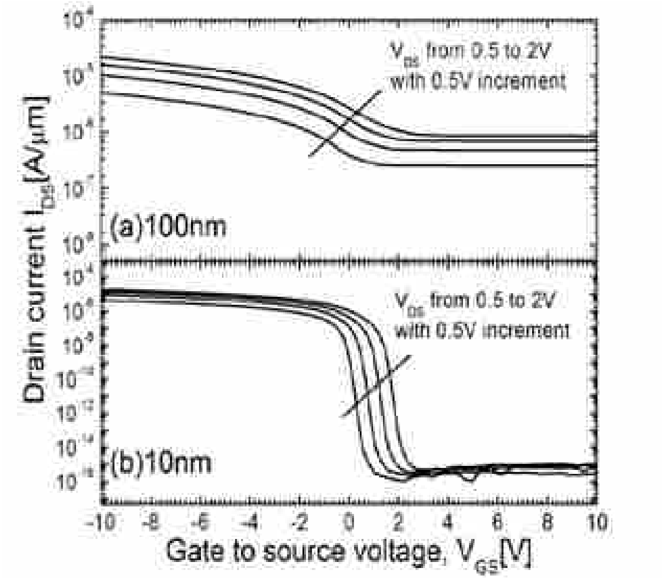

Figure 6.2: Transfer characteristics of p-type polysilicon nanowires with $10^{18}/cm^3$ doping concentration at different thicknesses; (a) 100nm and (b) 10nm.

Figure 6.2 shows transfer characteristics (I_{DS} vs V_{GS}) of p-type Si-NWs for different nanowire thicknesses while the doping density is $10^{18}/cm^3$. For the nanowire thickness of 100 nm in figure 6.2(a), the characteristics is severely degraded with a sub-threshold slope around 5246 mV/decade and a DIBL around 3220 mV/V. These drastically inferior sub-threshold characteristics render 100 nm thick polysilicon nanowire with a doping density of $10^{18}/cm^3$ unsuitable for a viable biosensor operation. However, for the nanowire thickness of 10 nm in figure 6.2(b), the sub-threshold characteristics are drastically changed. While sub-threshold characteristics of 100 nm thick nanowire with a doping of $10^{18}/cm^3$ is not promising for biosensor, the 10 nm thick polysilicon nanowire at this doping concentration exhibits a sub-threshold slope of 104 mV/decade and a DIBL around 1030 mV/V, which is quite comparable to the $10^{16}/cm^3$ doped nanowires and obviously promising for biosensor design. This result shows that a heavy doping around $10^{18}/cm^3$ can be used in biosensor design if nanowire thickness is scaled down to 10 nm or below. Low doped NW is traditionally used for biosensor design due to its extreme sensitivity which may allow single molecule analyte detection for early disease diagnosis. However, extreme sensitivity of NW also makes it vulnerable to noise as due to small size and large surface-to-volume ratio, minor perturbations at surface may deplete or accumulate the tiny volume of NW. As a result, to improve the signal to noise ratio in NW biosensor design, doping concentration may be required to be increased. It is apparent from figure. 6.1 and 6.2 that the doping concentration of nanowire cannot be increased arbitrarily. For viable biosensor performance, nanowire doping is inherently related to its thickness and if a design requires a doping around $10^{18}/cm^3$, then the thickness of the nanowire should be scaled down to 10 nm or below.

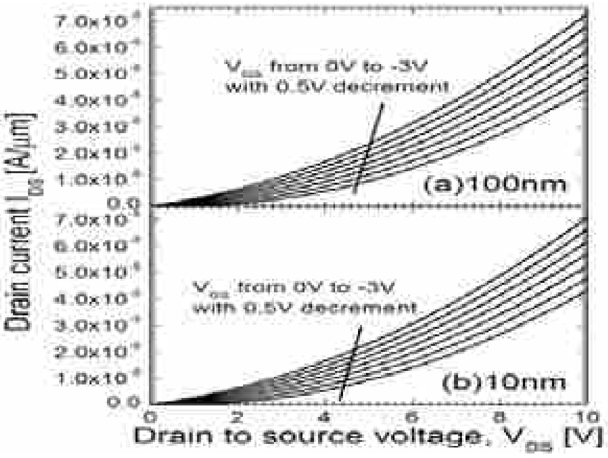

Figure 6.3: Output characteristics of p-type polysilicon nanowires with $10^{16}/cm^3$ doping concentration at different thicknesses; (a) 100nm and (b) 10nm.

Figure 6.3 shows output characteristics (I_{DS} vs. V_{DS}) of 10 µm long polysilicon nanowires for different nanowire thicknesses while the doping density is 10^{16}/cm^3. For the 100 nm thick nanowire in figure 6.3(a), I_{DS} vs V_{DS} characteristics is inherently non-linear at V_{Gs} = 0 V with a very low level of conduction up to 1.5 V of V_{DS} value in linear scale. This characteristic resembles the electrical characteristics observed in p-type silicon nanowires processed by wet anisotropic plane dependent etching by Chen et al [44]. Application of negative $V_{GS,}$ results in the increase of I_{DS} values which increases from 9.48 µA/µm at V_{GS} = 0V to 23.5 µA/µm at V_{GS} = -3 V for a V_{DS} = 5 V (60% change). This can be explained by the modulation of nanowire conduction due to strong hole accumulation upon application of the negative V_{GS} voltages. A similar characteristic can be observed for 10 nm thick nanowire (figure 6.3(b)). However, drive current of 10 nm thick nanowire is slightly lower than 100 nm thick nanowire and a similar change in the drive current can be observed for 10 nm thick polysilicon nanowire for a V_{GS} change from 0 to -3 V at V_{DS} = 5 V (60% change). This result implies that for a doping density of 10^{16}/cm^3, nanowire thickness scaling has mild effect on the electrical characteristics of polysilicon nanowires. This result also agrees with the result of figure 6.1 that is showing a non-phenomenological change of nanowires sub-threshold characteristics while thickness has been scaled from 100 nm to 10 nm at a doping density of 10^{16}/cm^3. As a result, it can be decided that thickness scaling of nanowires at the doping density of 10^{16}/cm^3 beyond 100 nm has no obvious benefit for biosensor operation and any nanowire thickness ranging from 100 nm to 10 nm can be chosen for biosensor design at this doping density.

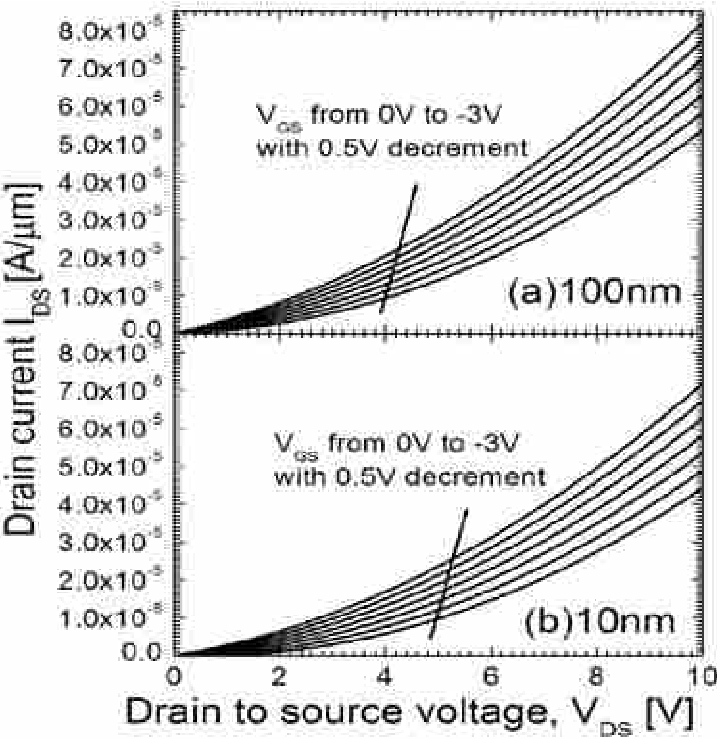

Figure 6.4: Output characteristics of p-type polysilicon nanowires with 10^{18}/cm^3 doping concentration at different thicknesses; (a) 100nm and (b) 10nm.

Figure 6.4 shows output characteristics (I_{DS} vs. V_{DS}) of 10 µm long polysilicon nanowires for different nanowire thicknesses while the doping density is 10^{18}/cm^3. In general, the I_{DS} vs. V_{DS} characteristics at 10^{18}/cm^3 is similar to 10^{16}/cm^3 doping density but the drive current is significantly increased. However, for the 100 nm thick nanowire (figure 6.4(a)), the drive current change for a V_{GS} change from 0 to -3 V at V_{DS} = 5 V is reduced to a value of 49% at a doping density of 10^{18}/cm^3 implying a less gate control on polysilicon nanowire at elevated doping level for 100 nm nanowire thickness. For the 10 nm thick nanowire at a doping density of 10^{18}/cm^3 (figure 6.4(b)), the drive current is slightly lower than 100 nm nanowire thickness. However, the drive current change for a V_{GS} change from 0 to -3 V at V_{DS} = 5 V is around 60% which is much higher than 100 nm nanowire thickness at a doping density of 10^{18}/cm^3 and similar to the drive current change found for 10^{16}/cm^{3}doping density. This result agrees with figure 3 and implies that for a doping around 10^{18}/cm^3, the thickness of the nanowire should be scaled down to 10 nm or below for a viable biosensor operation.

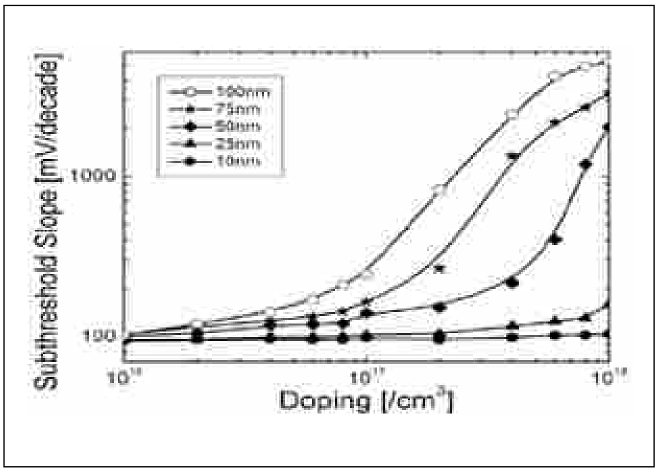

Figure 6.5: Sub-threshold slopes as a function doping concentrations for different thicknesses of polysilicon nanowires.

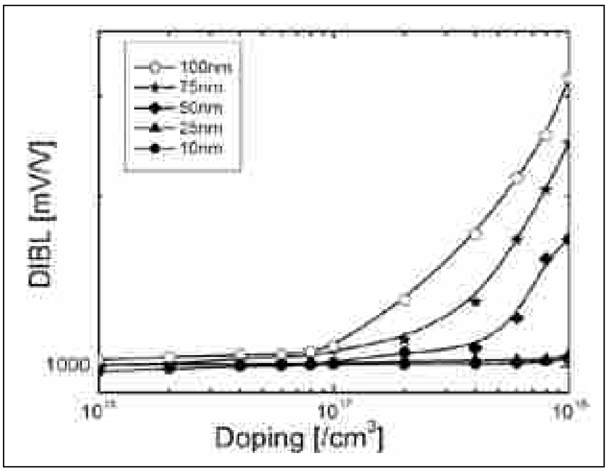

Figure 6.6: Drain induced barrier lowering (DIBL) as a function doping concentrations for different thicknesses of polysilicon nanowires.

To elucidate the proper combination of nanowire thickness and doping to ensure the sensitive operation of polycrystalline silicon nanowire biosensors, figure. 6.5 summarizes the extracted values of sub-threshold slopes as a function doping concentrations for different thicknesses of polysilicon nanowires. For nanowire thicknesses of 100 nm and 75 nm, a severely degraded sub-threshold slope can be observed when doping concentrations are above 10^{17}/cm^3. The polysilicon nanowires exhibit sub-threshold slopes of 5246 mV/dec and 3344 mV/dec respectively for 100 nm and 75 nm nanowire thicknesses at a doping concentration of 10^{18}/cm^3. A plausible sub-threshold slope around 100 mV/dec for a viable biosensor operation at these thicknesses can only be achieved if doping concentration is 2×10^{16}/cm^3 or below. For a 50 nm nanowire thickness, a relatively wide doping concentration range can be chosen for biosensor design while maintaining decent sub-threshold characteristics. In this thickness a doping up to 4×10^{17}/cm^3 with a sub-threshold slope around 100 mV/dec can be chosen. The widest range of doping concentrations can be chosen for 25 nm and 10 nm nanowire thicknesses with a maximum doping up to 10^{18}/cm^3 while maintaining a promising sub-threshold slope around 95 mV/dec for a viable biosesnsor design using polycrystalline silicon nanowires. Finally, figure 6.7 summarizes the extracted values of drain induced barrier lowering (DIBL) as a function doping concentrations for different thicknesses of polysilicon nanowires. The DIBL trend of polysilicon nanowires is similar to the observed sub-threshold slopes at different doping concentrations and nanowire thicknesses (figure 6.6) and show the plausible combinations of doping concentrations and nanowire thicknesses for polycrystalline silicon nanowire biosensor fabrication.

DISCUSSION

We have investigated the effect of nanowire thickness and doping concentration on the electrical characteristics of polycrystalline silicon nanowire biosensors. For nanowire thicknesses of 100 nm and 75 nm, a plausible sub-threshold slope around 100 mV/dec for a viable biosensor operation can only be achieved if doping concentration is 2×10^{16}/cm^3 or below. For a 50 nm nanowire thickness a relatively wide doping concentration range with a maximum doping up to 4×10^{17}/cm^3 can be chosen for biosensor design while maintaining decent sub-threshold characteristics. The widest range of doping concentrations can be chosen for 25 nm and 10 nm nanowire thicknesses with a maximum doping up to 10^{18}/cm^3 while maintaining a promising sub-threshold slope around 95 mV/dec for a viable biosesnsor design using polycrystalline silicon nanowires. As such this research reveals the possible combinations of nanowire thickness and doping to ensure the sensitive operation of polycrystalline silicon nanowire biosensors.

CHAPTER 7

7. COMPARATIVE SENSOR PERFORMANCE OF POLYSILICON AND SINGLE CRYSTAL SILICON NANOWIRE BIOSENSORS:

Figure 7.1 shows sub-threshold characteristics (I_{DS}vs V_{GS}) of p-type (single crystal and poly crystal) Si NWs for 100nm nanowire thickness. The length of the nanowire is 1µm and doping density is $10^{16}/cm^3$. For single crystal Si in Figure 7.1, the sub-threshold slope is found to be 105mV/decade. The drive current of single crystal Si NW is found to be 1.23*10^{-4}A/µm at V_{DS}= 0.5V and V_{GS}= -5V. For poly Si NW sub threshold slope S is found to be 113mv/decade. The sub threshold slope of 1µm long 100nm thick poly Si NW is inferior to that of the single crystal Si NW. The drive current is also lower than single crystal Si NW with a value of 2.11*10^{-5}A/µm at V_{DS}= 0.5V and V_{GS}= -5V. Although the exhibited value of sub threshold slope is higher than ideal 60 mV/decade; a sub-threshold swing around100 mv/decade is fair for using both poly Si and single crystal Si NW as sensors with slightly degraded performances for poly Si case.

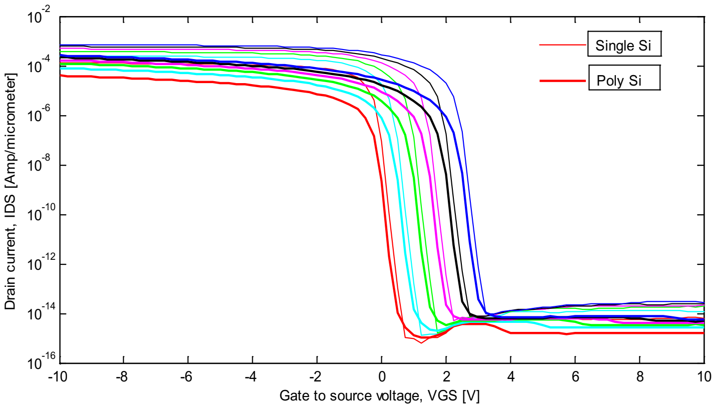

Figure 7.1: Sub-threshold characteristics of p-type Silicon nanowires with $10^{16}/cm^3$ doping concentration at 100nm thickness; (a) single crystal Si and (b) poly crystal Si. The NWs have channel length of 1µm.

Figure 7.2 shows output characteristics (I_{DS} vs. V_{DS}) of 1µm long p-type (single crystal and poly crystal) silicon nanowires for 100nm thickness while the doping density is $10^{16}/cm^3$. For single crystal Si NW, a typical non-

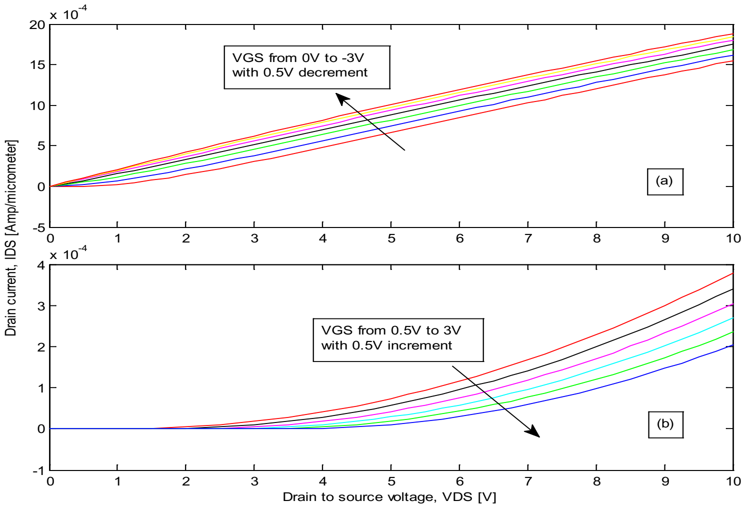

Figure 7.2: Output characteristics of p-type Silicon nanowires with $10^{16}/cm^3$ doping concentration at 100nm thickness; (a) single crystal Si and (b) poly crystal Si.The NWs have channel length of 1µm.

linear characteristics is observed with insignificant conduction up to certain level of drain bias. With the application of negative V_{GS} this non-linear characteristics is reduced and drive current increases. The increase in drive current can be explained by the modulation of NW conduction due to strong hole accumulation upon application of negative $V_{GS.}$ For poly Si NW the non-linearity of I_{DS}-V_{DS} characteristics is significantly increased. In particular the NWs drive current is significantly lower and the NWs do not show significant conduction up to 2V of $V_{DS.}$

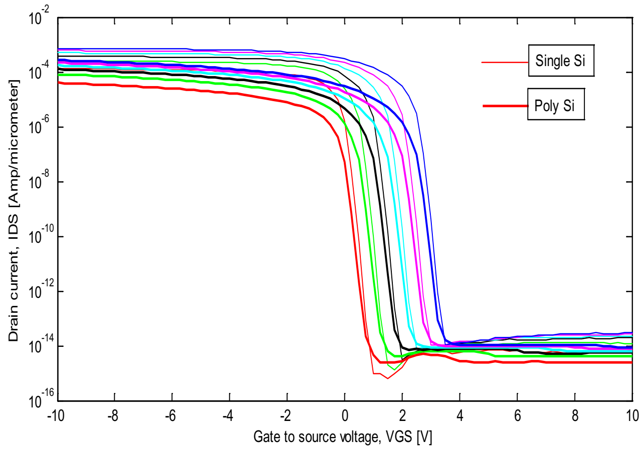

Figure 7.3: Sub-threshold characteristics of p-type Silicon nanowires with $4*10^{17}/cm^3$ doping concentration at 100nm thickness; (a)single crystal Si and (b) poly crystal Si.The NWs have channel length of 1µm.

Figure 7.3 shows sub-threshold characteristics (I_{DS}vs. V_{GS}) of p-type (single crystal and poly crystal) Si NWs for 100nm nanowire thickness. The length of the nanowire is 1µm and doping density is $4*10^{17}/cm^3$. For single crystal Si in Figure 7.3 (a), the sub-threshold slope is found to be 2420mV/decade. And for the poly crystal Si in Figure 7.3 (b), the sub-threshold slope is found to be 2530mV/decade. These drastically inferior sub-threshold characteristics of single and poly-silicon nanowires with a doping density of $4*10^{17}/cm^3$makes 100nm thick nanowire unsuitable for a viable biosensor operation. Although the sub-threshold slope of single crystal Si is lower than the poly crystal Si, both have very high values of slopes than the ideal value. This observation implies that both single and poly crystal Si nanowire cannot be used as sensor with a doping density of $4*10^{17}/cm^3$. The drive current of single crystal Si NW is $1.6*10^{-4}$A/µm at V_{GS}=-5V and V_{DS}=0.5V. This current is again higher than poly Si NW which has a value of $2.27*10^{-5}$A/µm as this is biasing condition.

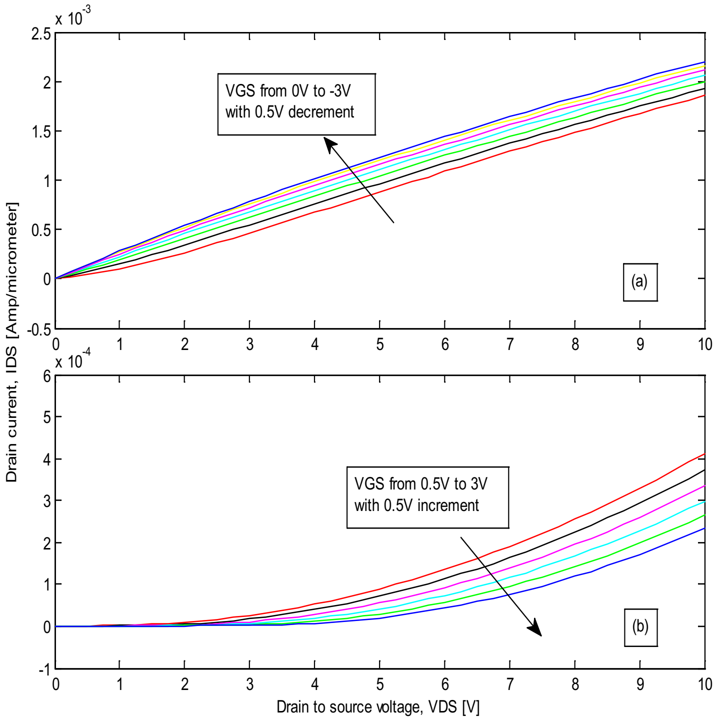

Figure 7.4: Output characteristics of p-type Silicon nanowires with $4*10^{17}/cm^3$ doping concentration at 100nm thickness; (a) single crystal Si and (b) poly crystal Si.The NWs have channel length of 1µm.

Figure 7.4 shows output characteristics (I_{DS} vs. V_{DS}) of 1µm long p-type (single crystal and poly crystal) silicon nanowires for 100nm thickness while the doping density is $4*10^{17}/cm^3$. For single crystal Si NW, the characteristics is more linear at this doping density in comparison to the doping of $10^{16}/cm^3$ and the typical (Figure 7.2(a)) non-conduction region also disappears. However, for poly Si NW the characteristics is still non-linear with an insignificant conduction up to a $V_{DS} = 2$V. The drive current of poly Si NW is inferior to single crystal Si NW. However, both single crystal Si and poly Si NW at this doping exhibit higher drive current than 10^{16} /cm^3 doping density (Figure 7.2).

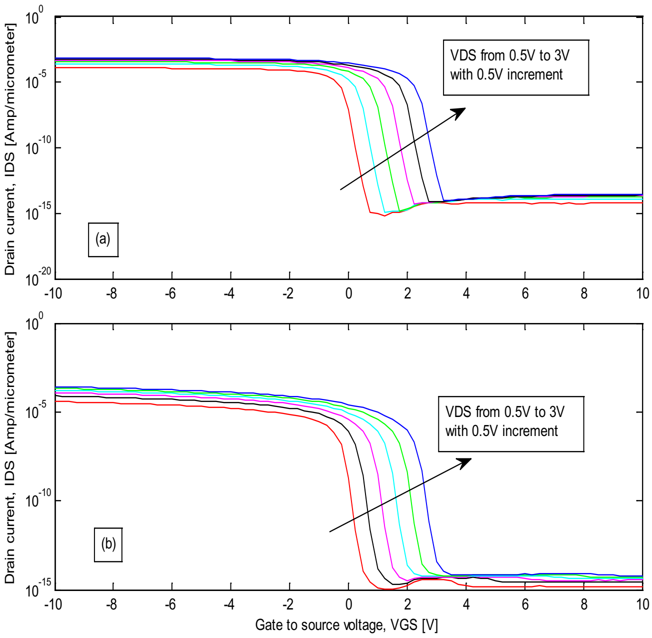

Figure 7.5: Sub-threshold characteristics of p-type Silicon nanowires with 10^{16}/cm^3 doping concentration at 25nm thickness; (a) single crystal Si and (b) poly crystal Si.The NWs have channel length of 1μm.

Figure 7.5 shows sub-threshold characteristics (I_{DS} vs. V_{GS}) of p-type (single crystal and poly crystal) Si NWs for 25nm nanowire thickness. The length of the nanowire is 1μm and doping density is 10^{16}/ cm^3. For single crystal Si in Figure 7.5 (a), the sub-threshold slope is found to be 86.1 mV/decade which is noticeably better than the 100nm thick single crystal Si NW at doping of 10^{16}/ cm^3. The drive current of single crystal Si NW is $1.14*10^{-4}$A/μm at V_{DS} = 0.5V and V_{GS}= -5V which is lower than 100nm thick single crystal Si NW at this doping (Figure 3.1). For poly Si sub threshold, slope is 103mV/decade which is inferior than single crystal Si NW at this doping. However, poly Si NWs sub-threshold slope at 25nm thickness is found to be improved in comparison to the 100nm thickness (Figure 3.1).

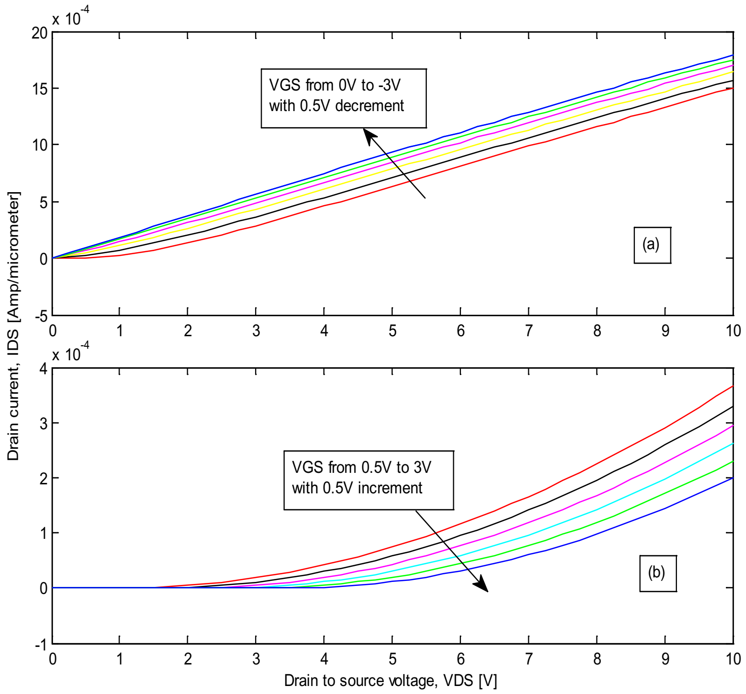

Figure 7.6: Output characteristics of p-type Silicon nanowires with 10^{16}/ cm^3 doping concentration at 25nm thickness; (a)single crystal Si and (b) poly crystal Si.The NWs have channel length of 1μm.

Figure 7.6: shows output characteristics (I_{DS} vs. V_{DS}) of 1μm long p-type (single crystal and poly crystal) silicon nanowires for 25nm thickness while the doping density is 10^{16}/cm^3. For single crystal Si NW, the output characteristics at 25nm thickness and 10^{16} /cm^3 doping is similar to that of 100nm thick NW at this doping. However, the drive current of poly Si NW at 25nm thickness is lower than 100nm thickness. For poly Si NW (Figure 7.6(b)) the characteristics is again more non-linear than single crystal Si NW which is similar to the observations of NW's output characteristics at doping 10^{16} /cm^3 and 100nm thickness.

Figure 7.7 shows sub-threshold characteristics (I_{DS} vs. V_{GS}) of p-type (single crystal and poly crystal) Si NWs for 25nm nanowire thickness. The length of the nanowire is 1μm and doping density is $4*10^{17}/cm^3$. A drastic change in the NW characteristics can be observed for 25nm thick Si NW at this doping density. While 100nm thick NW at doping of $4\times10^{17}/cm^3$ exhibited significantly unsuitable sub-threshold slope for sensor operation, 25nm thick nanowire exhibited significantly improved sub-threshold slope value at doping of $4\times10^{17}/cm^3$. The sub threshold slope of single crystal and poly crystal Si NWs are 97.9mV/decade and 118mV/decade respectively which is much better than 100nm thick NW's at this doping (Figure 7.3). It should also be noted that the drive current of poly/single crystal NWs at this doping is higher than $10^{16}/cm^3$ doping.

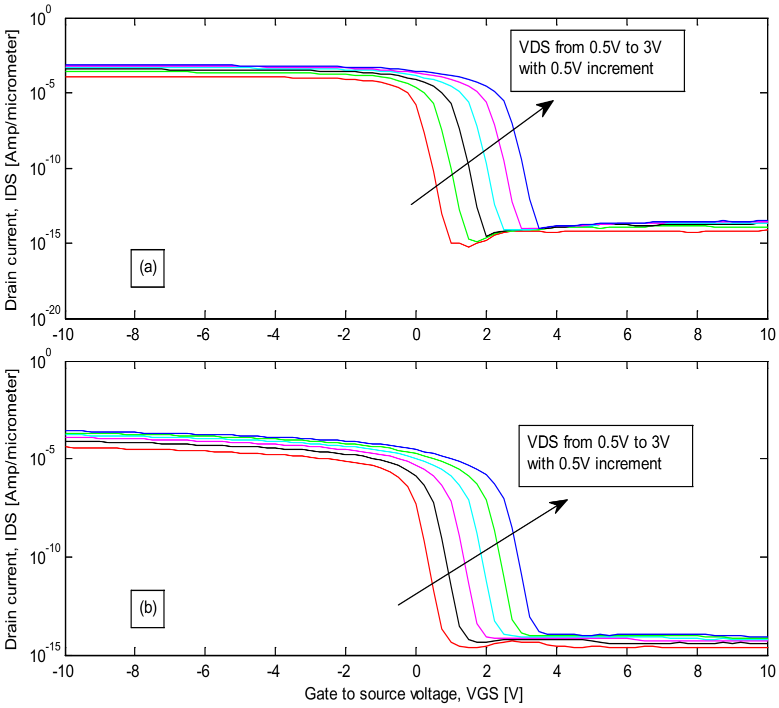

Figure 7.7: Sub-threshold characteristics of p-type Silicon nanowires with $4*10^{17}/cm^3$ doping concentration at 25nm thickness; (a) single crystal Si and (b) poly crystal Si.The NWs have channel length of 1μm.

Figure 7.8 shows output characteristics (I_{DS} vs. V_{DS}) of 1μm long p-type (single crystal and poly crystal) silicon nanowires for 25nm thickness while the doping density is $4*10^{17}/cm^3$. The exhibited output characteristics are similar to the output characteristics observed previously for 100nm NW thickness at this doping. Except that the drive current is lower than 100nm thick NW's at this doping (Figure7.4).

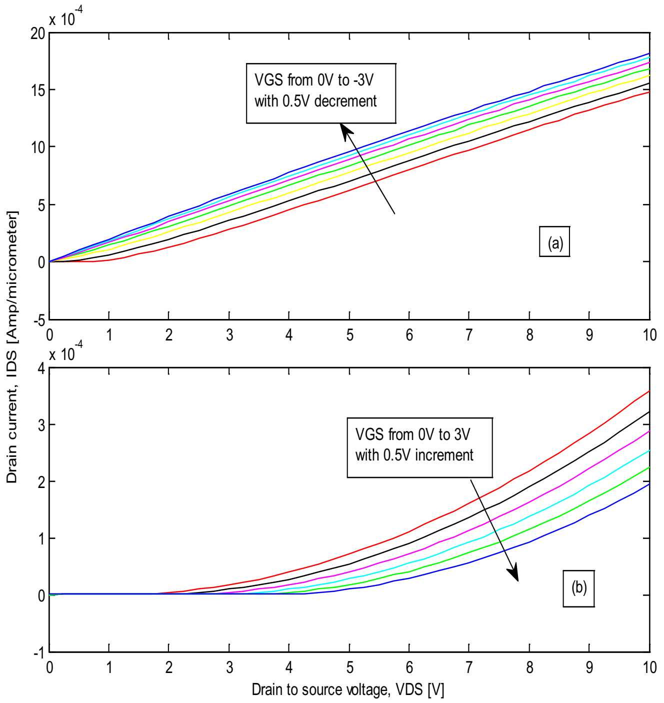

Figure 7.8: Output characteristics of p-type Silicon nanowires with $4*10^{17}/cm^3$ doping concentration at 25nm thickness; (a) single crystal Si and (b) poly crystal Si.The NWs have channel length of 1μm.

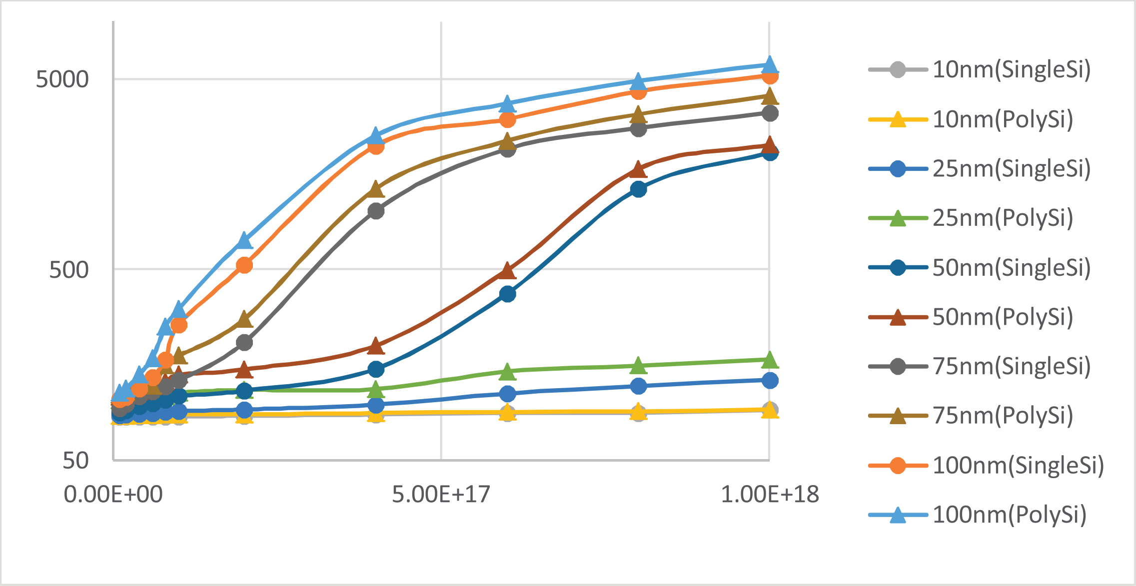

Figure 7.9: Sub-threshold slopes as a function of doping concentrations for different thicknesses of single crystal Silicon and poly crystal Silicon nanowires.

Figure 7.9 summarizes the extracted values of sub-threshold slopes as a function of doping concentrations for different thicknesses & for single crystal silicon / poly crystal silicon nanowires. It can be seen that poly Si NW generally shows inferior characteristics than single crystal Si NW at all doping densities for NW thicknesses of 100, 75, 50 & 25nm which agrees well with general belief that poly Si NW will give inferior sensor performance than single crystal Si NW. However, for 10nm Si NW single crystal & poly Si, NW show some sub-threshold slopes at all doping densities. Considering thecheap & mass manufacturable platform of poly Si material, it can be decided that poly Si NW biosensor with Si thickness ≤ 10nm is the possible commercial route of sensor fabrication. Figure 7.9 also elucidates the proper combination of nanowire thickness and doping to ensure the sensitive operation of single crystal and polycrystalline silicon nanowire biosensors. For nanowire thickness of 100nm and 75nm, a severely degraded sub threshold slope can be observed when doping concentration are above 10^{17} /cm^3 both for single crystal and poly Si nanowires. The polysilicon nanowires exhibit sub-threshold slopes of 5970mV/decade and 4080mV/decade respectively for 100nm and 75nm nanowire thickness at the doping concentration of 10^{18}/cm^3. The single crystal Si NWs exhibit sub-threshold slopes of 5220mV/decade and 3330mV/decade respectively for 100nm and 75nm nanowire thickness at a doping concentration of 10^{18} /cm^3 . A plausible sub threshold slope around 100 mV/decade for a viable biosensor operation at these thickness can only be achieve if doping concentration is 2*10^{16}/cm^3 or below both for single crystal and poly silicon nanowires. For a 50nm nanowire thickness, a relatively wide doping concentration range can be chosen for biosensor design while maintaining decent sub threshold characteristics. In this thickness a doping up 4*10^{17}/cm^{3}with asub-threshold slope around 100 mV/decade can be chosen. The widest range of doping concentrations can be chosen for 25nm and 10nm nanowire thickness with a maximum doping up to 10^{18}/cm^{3}while maintaining a promising sub threshold slope around 95mV/decade for a viable biosensor design using both single and polycrystalline silicon nanowires.

CHAPTER 8

8. CONCLUSIONS

We have investigated the effect of nanowire thickness and doping concentration on the electrical characteristics of single crystal and polycrystalline silicon nanowire biosensors. For nanowire thicknesses of 100 nm and 75 nm, a plausible sub-threshold slope around 100 mV/decade for a viable biosensor operation can only be achieved if doping concentration is $2*10^{16}/cm^3$ or below both for single crystal and poly Si nanowires. For a 50nm nanowire thickness, a relatively wide doping concentration range with a maximum doping up to $4*10^{17}/cm^3$ can be chosen for biosensor design while maintaining decent sub-threshold characteristics. The widest range of doping concentrations can be chosen for 25nm and 10nm nanowire thickness with a maximum doping up to $10^{18}/cm^3$ while maintaining a promising sub-threshold slope around 95 mV/decade for a viable biosensor design using single crystal and polycrystalline silicon nanowires.In general, poly Si NW shows inferior characteristics than single crystal Si NW. However, for 10nm Si NW single crystal & poly Si NW show same sub-threshold slopes at all doping densities. It can be decided from this work that poly Si NW biosensor with Si thickness ≤ 10nm is the possible commercial route of sensor fabrication.

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GENERATED DATASET FOR ASSESSING THE PERORMANCE OF SINGLE CRYSTAL SILICON NANOWIRE BIOSENSOR

APPENDIX A: TRANSFER CHARACTERISTICS

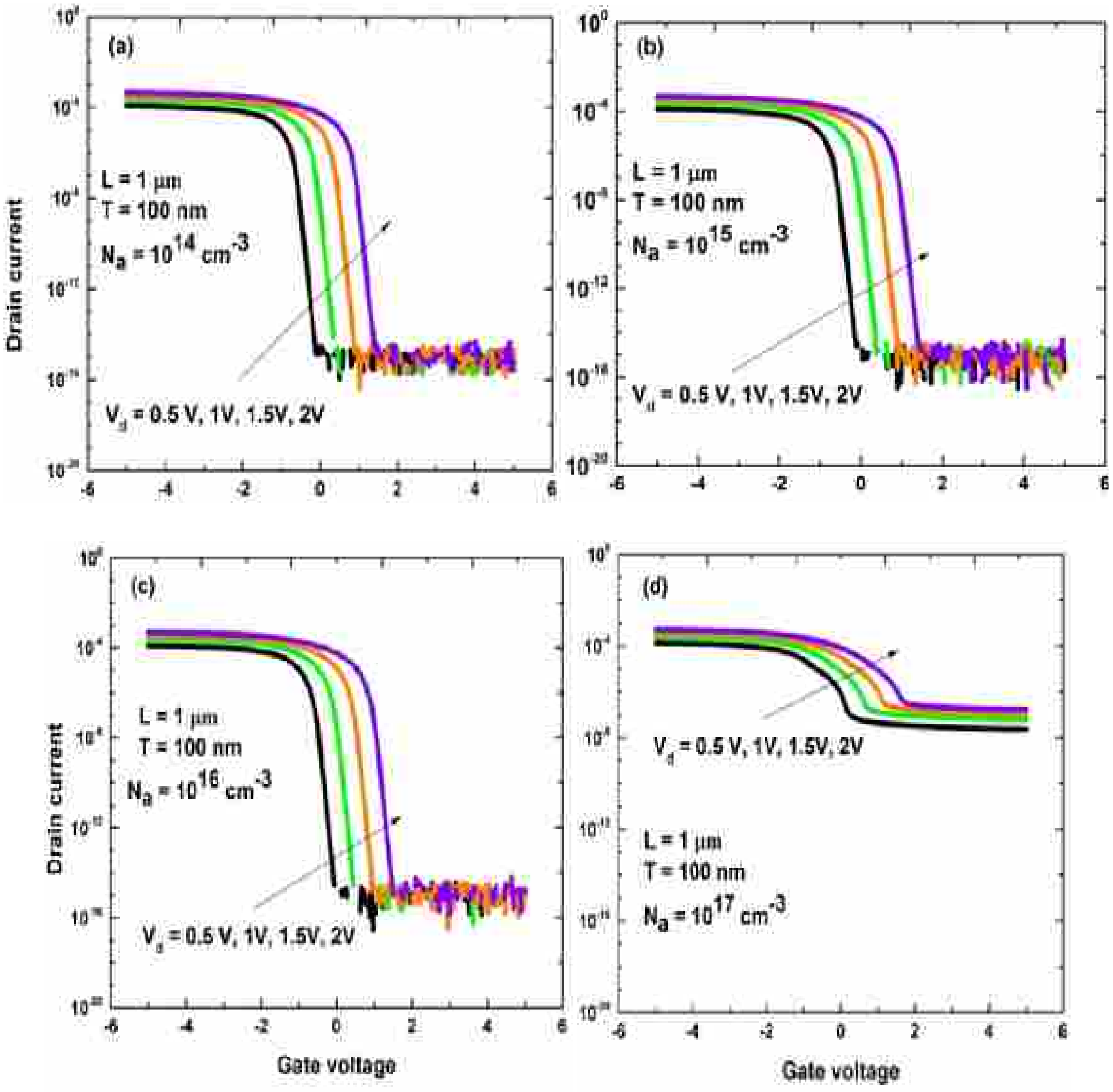


Figure A.1: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1µm. *(Continued to next page)*.

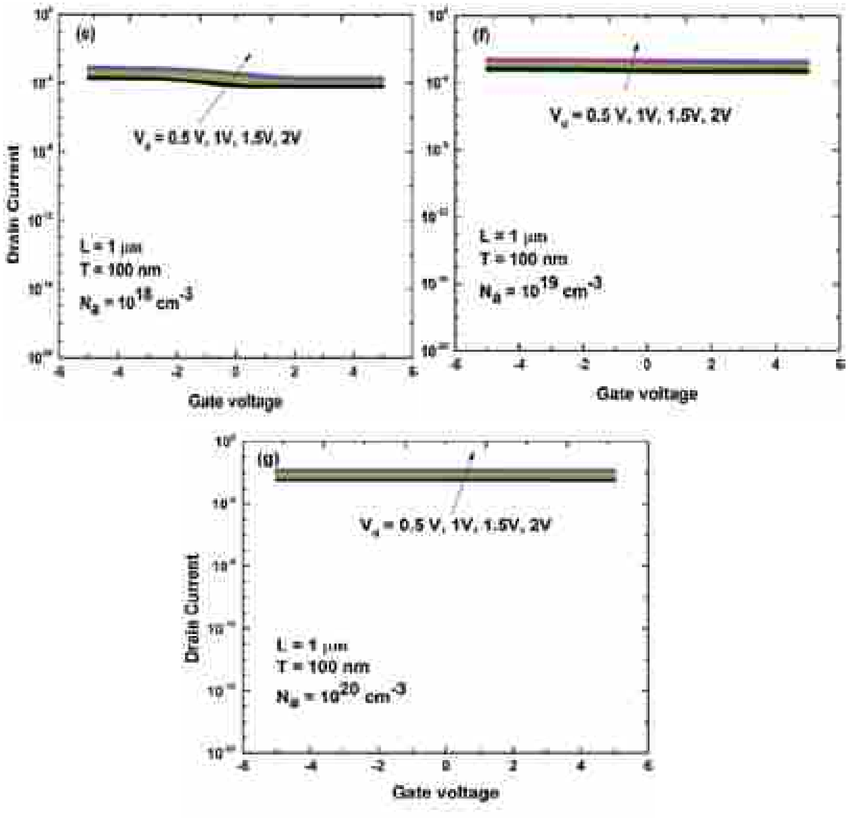


Figure A.1: ***(Continued)*** **Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.**

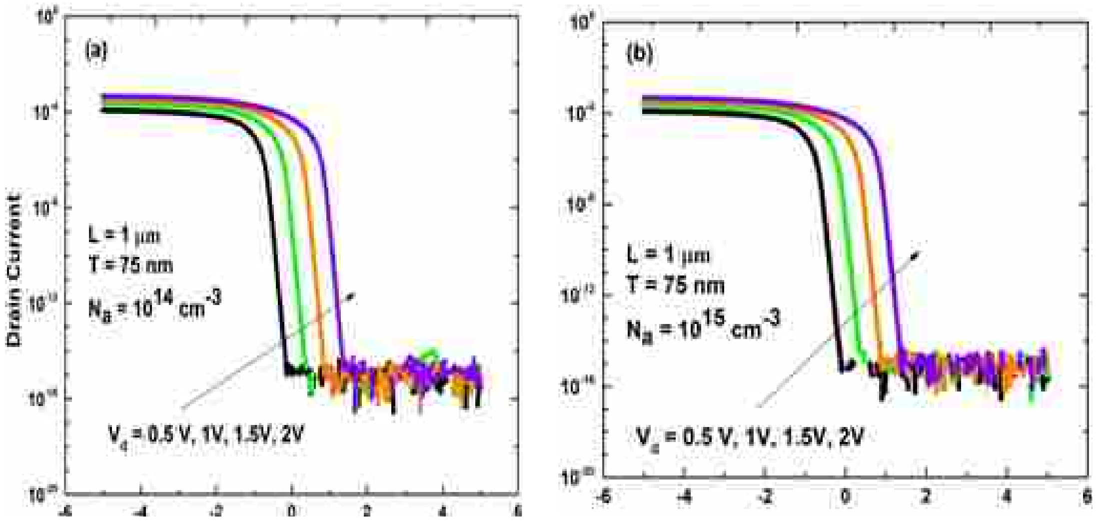


Figure A.2: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 75nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. ***(Continued to next page).***

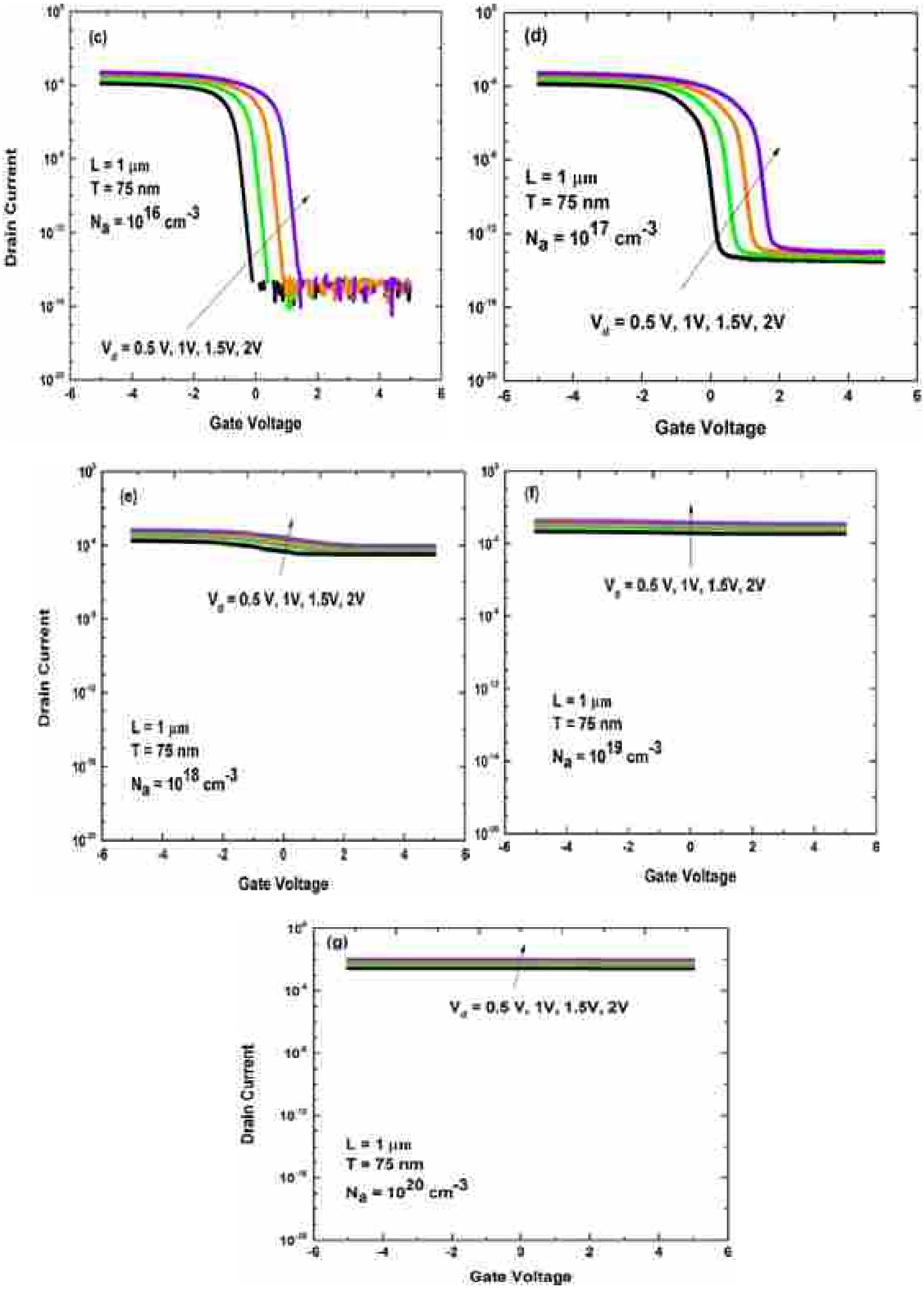


Figure A.2: ***(Continued)*** **Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 75nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm**

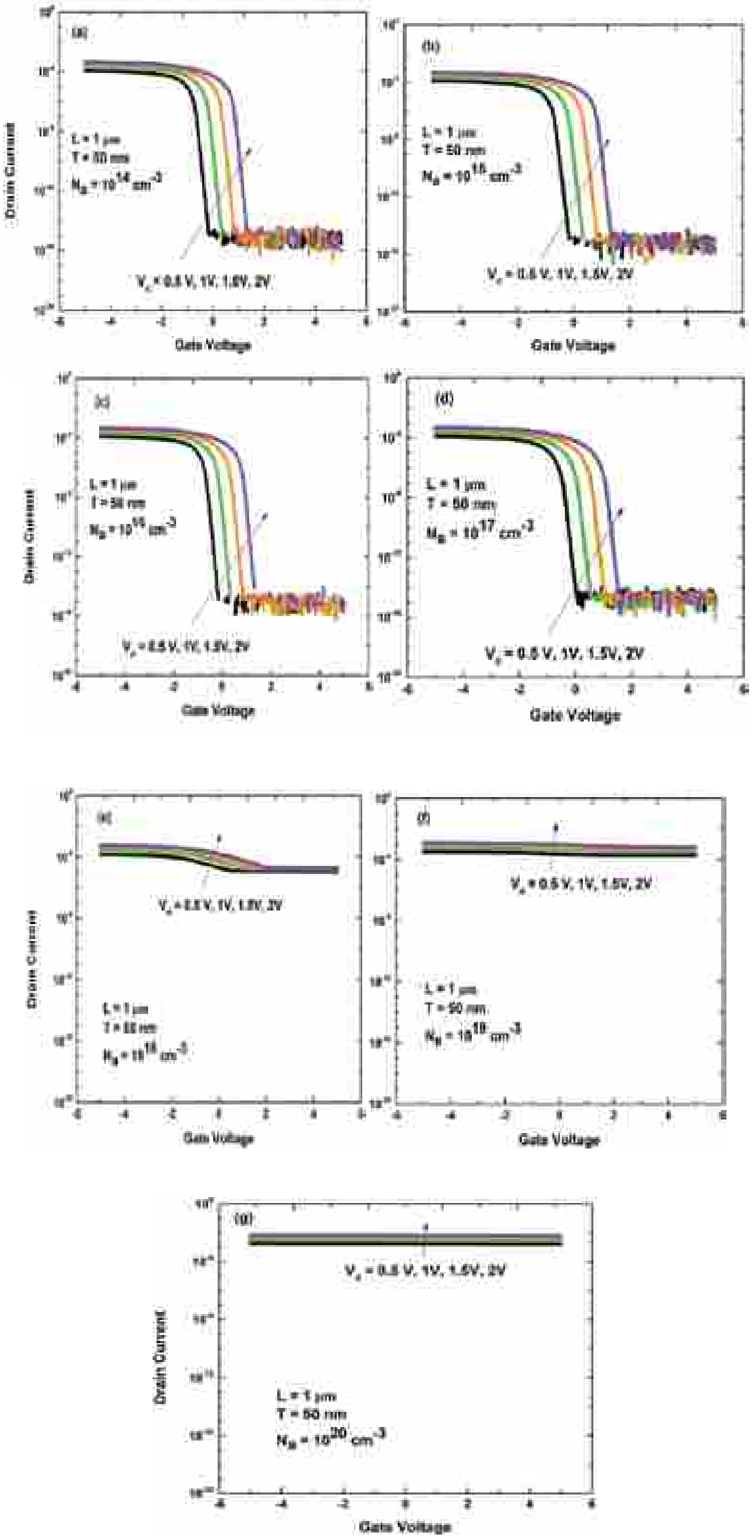


Figure A.3: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 50nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

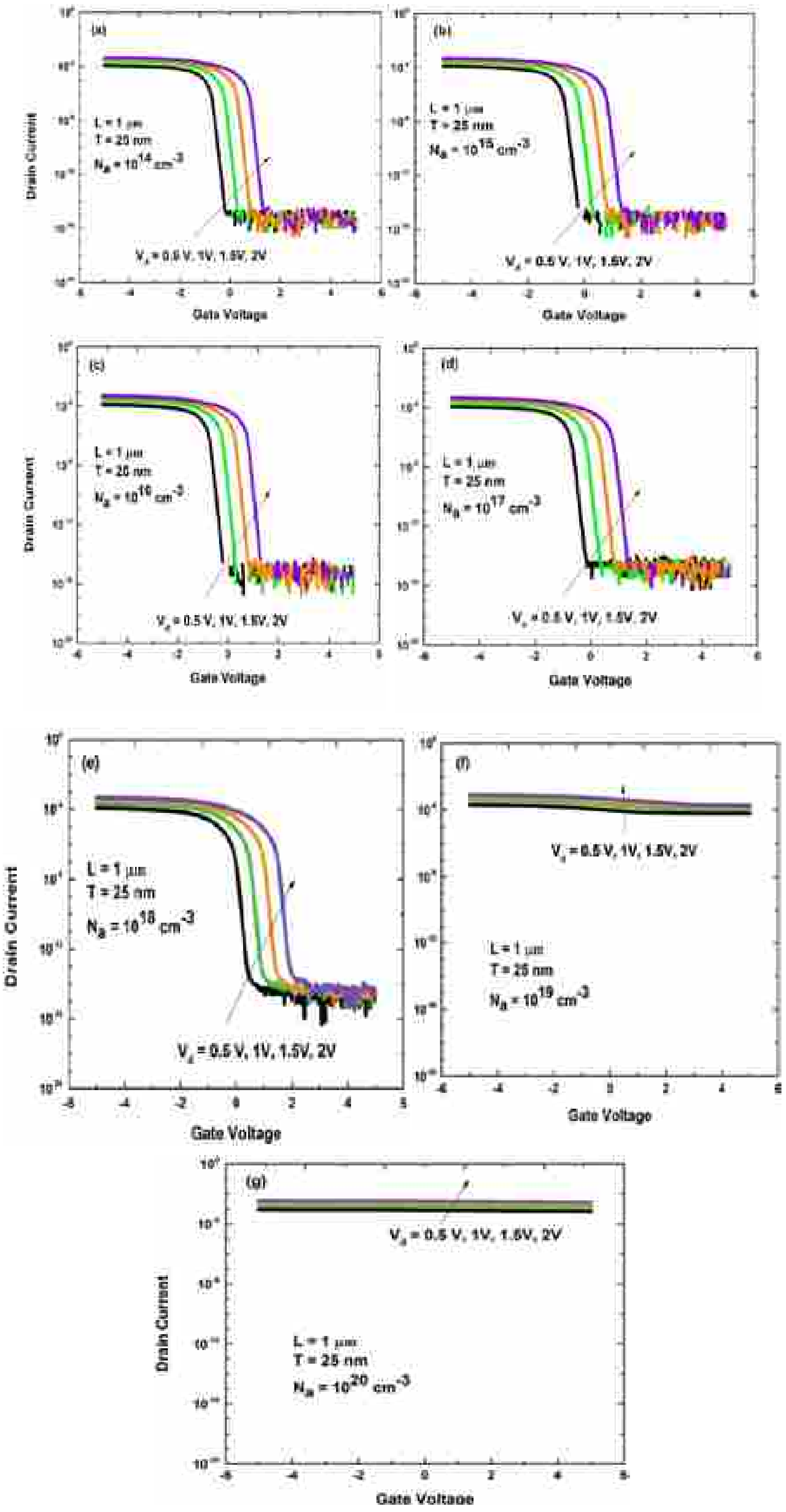


Figure A.4: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 25nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1µm.

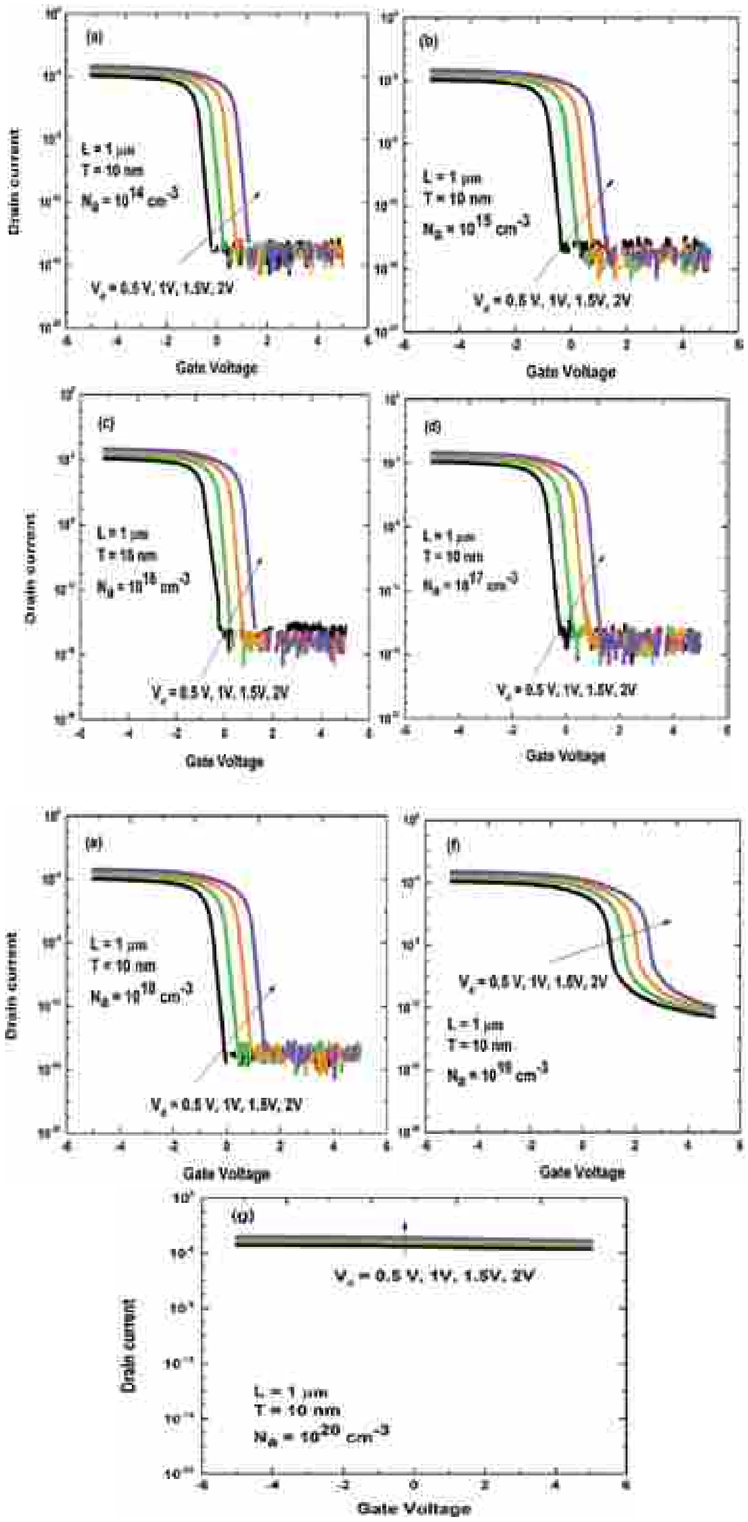


Figure A.5: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 10nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

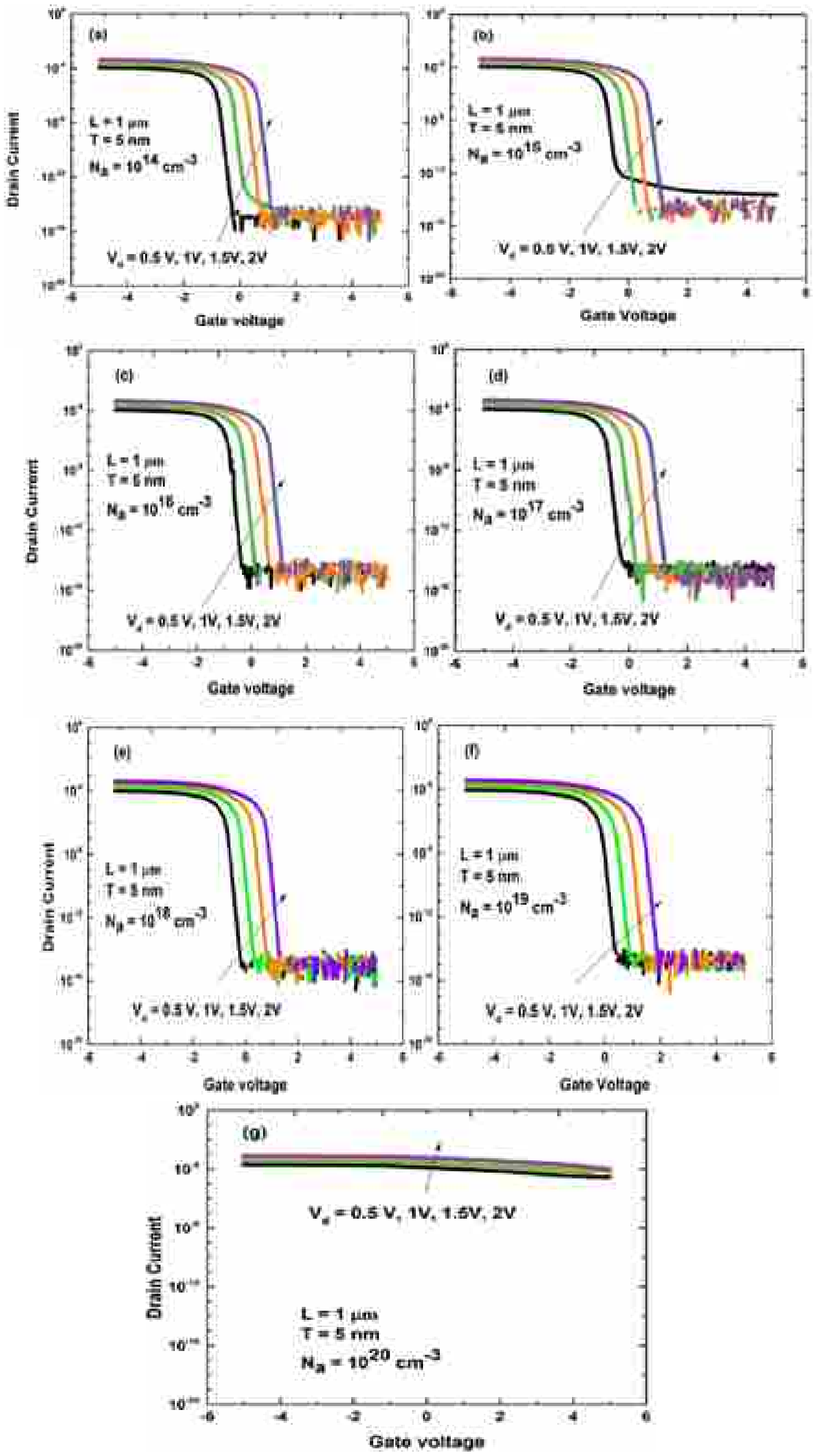


Figure A.6: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1µm.

APPENDIX B: OUTPUT CHARACTERISTICS

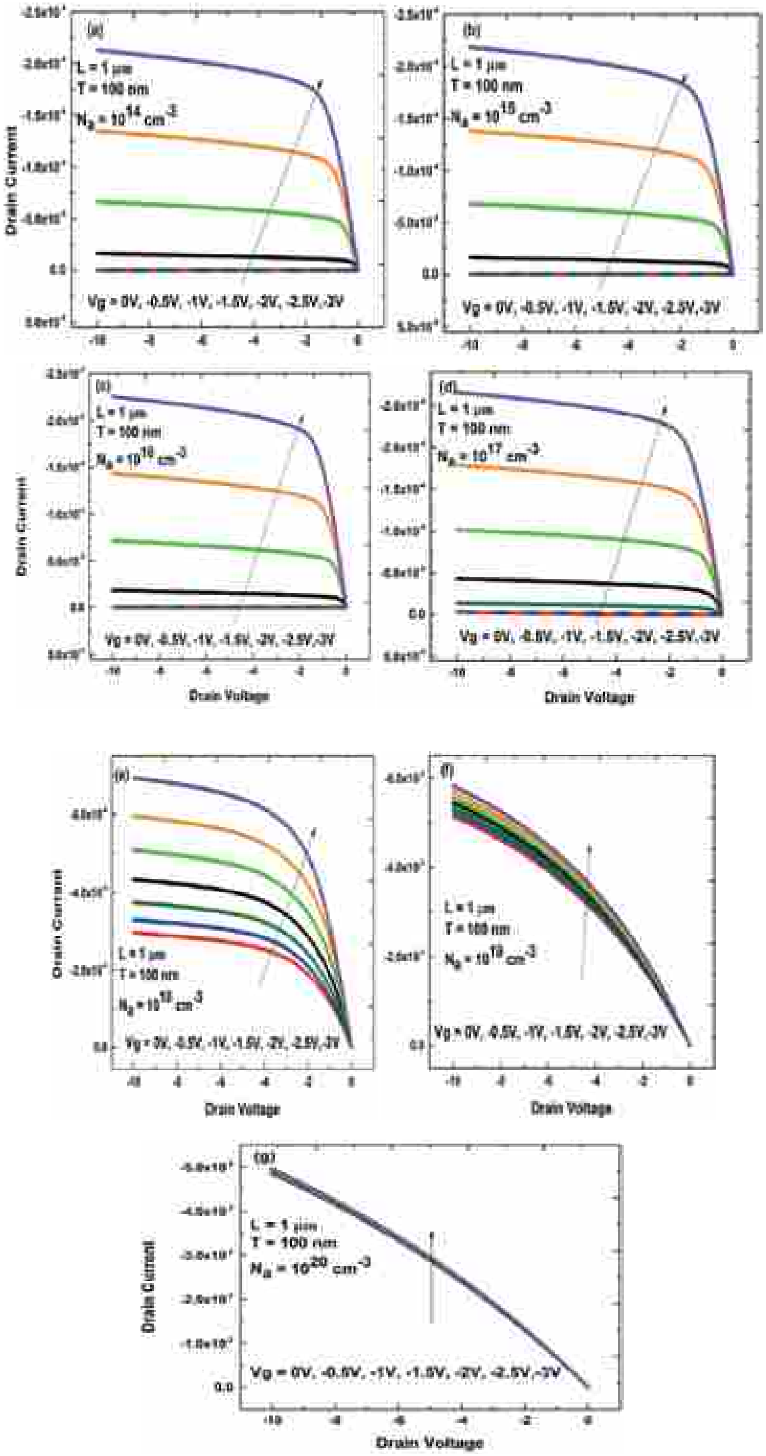


Figure B.1: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

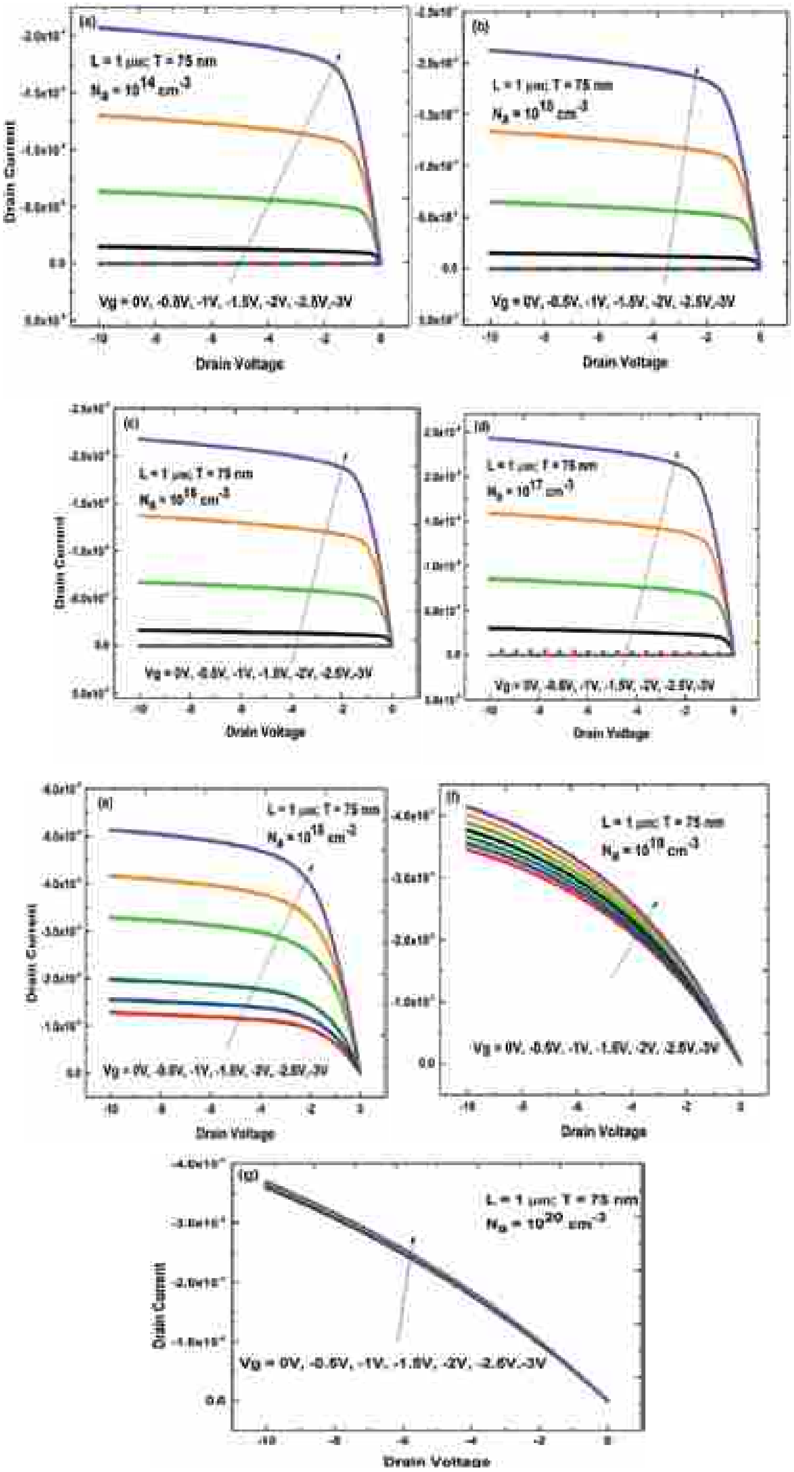


Figure B.2: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 75 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

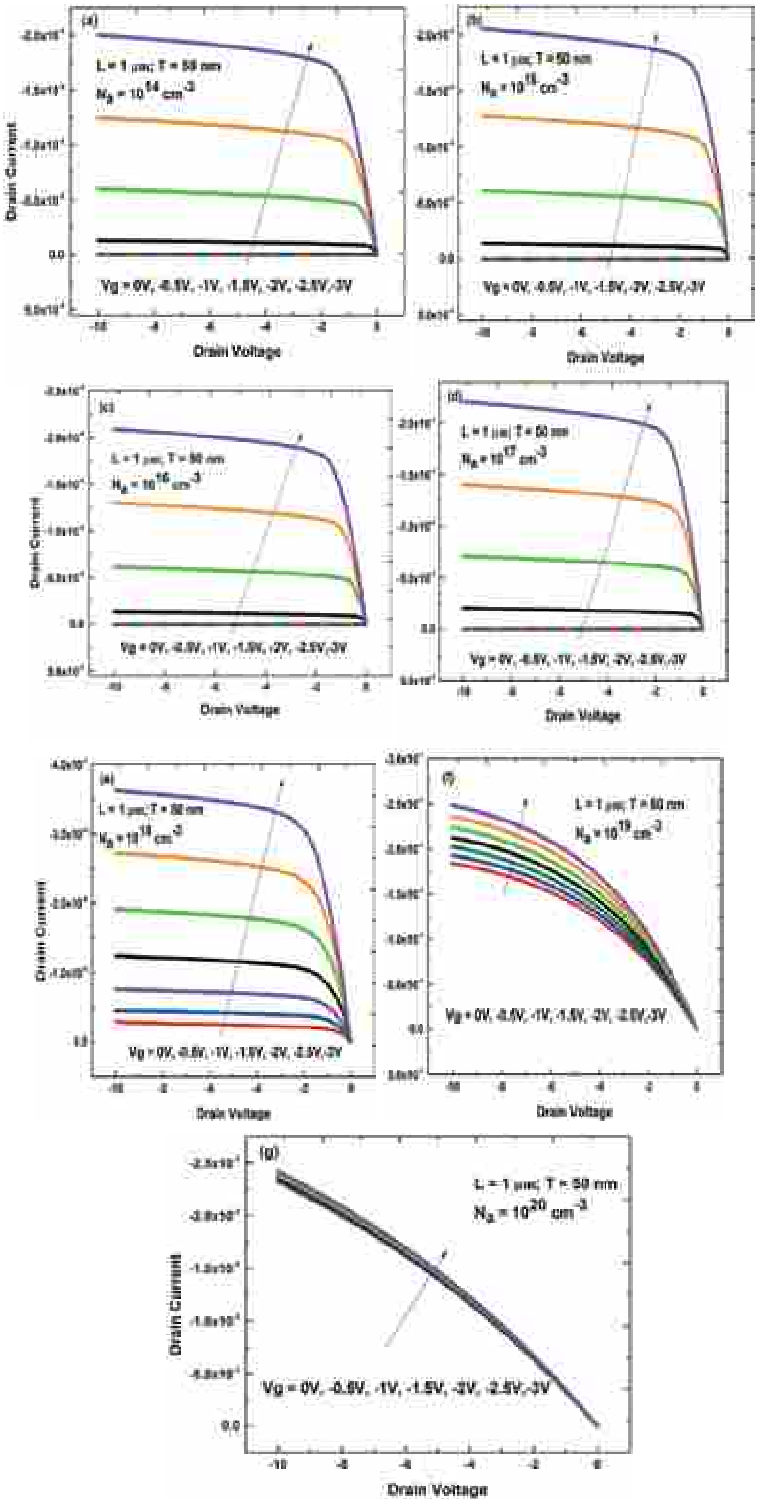


Figure B.3: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 50 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1µm.

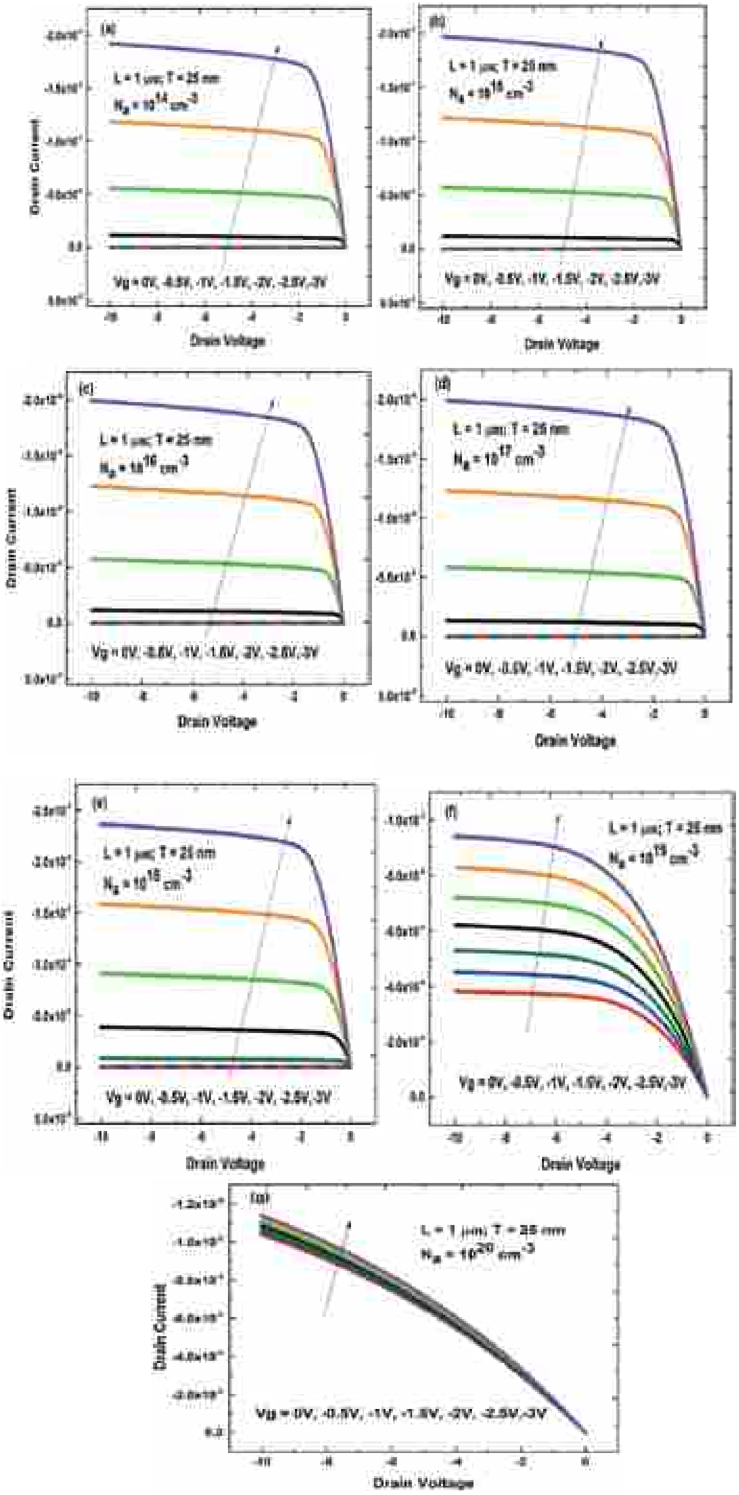


Figure B.4: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 25 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1µm.

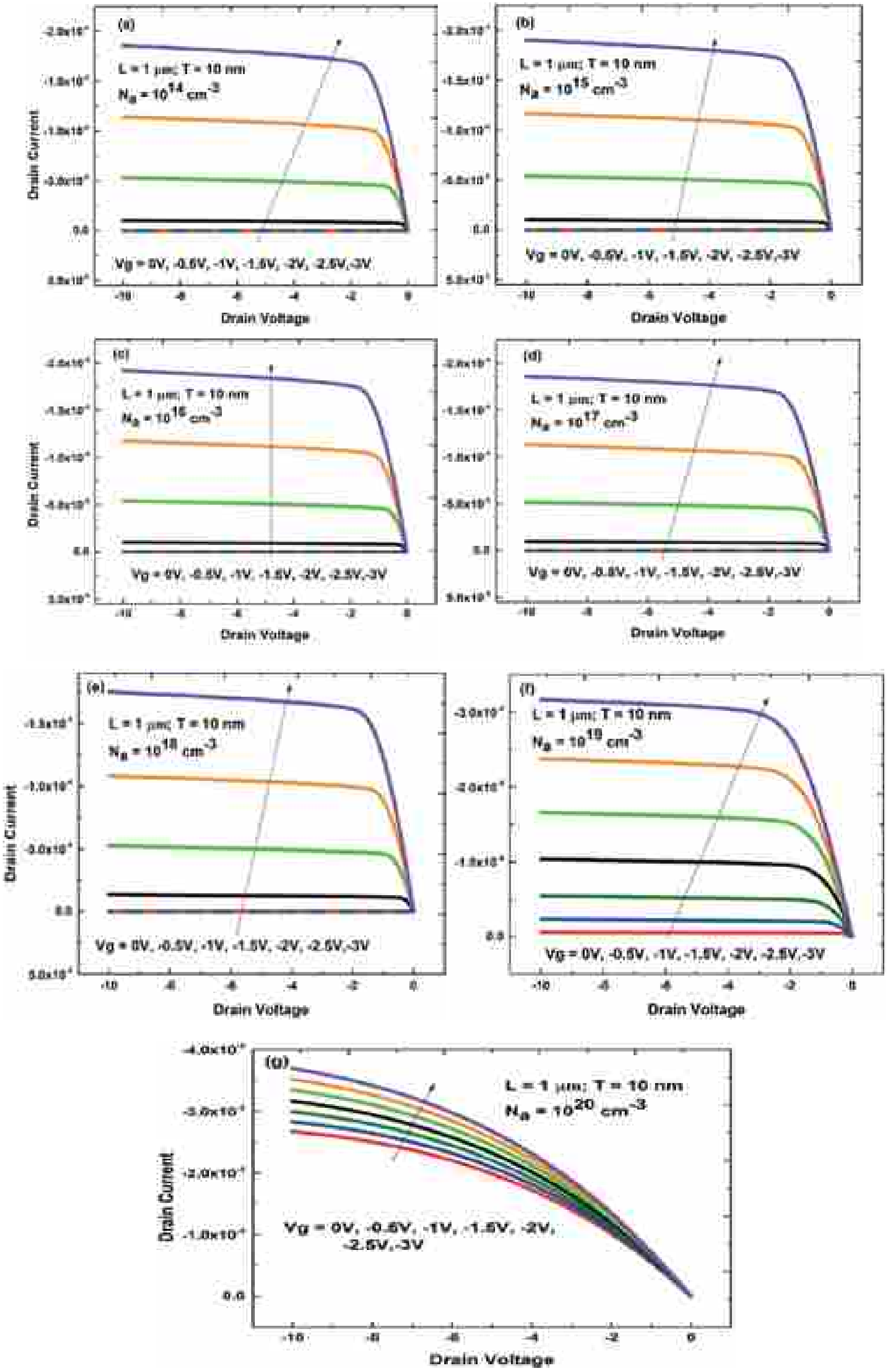


Figure B.5: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 10 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

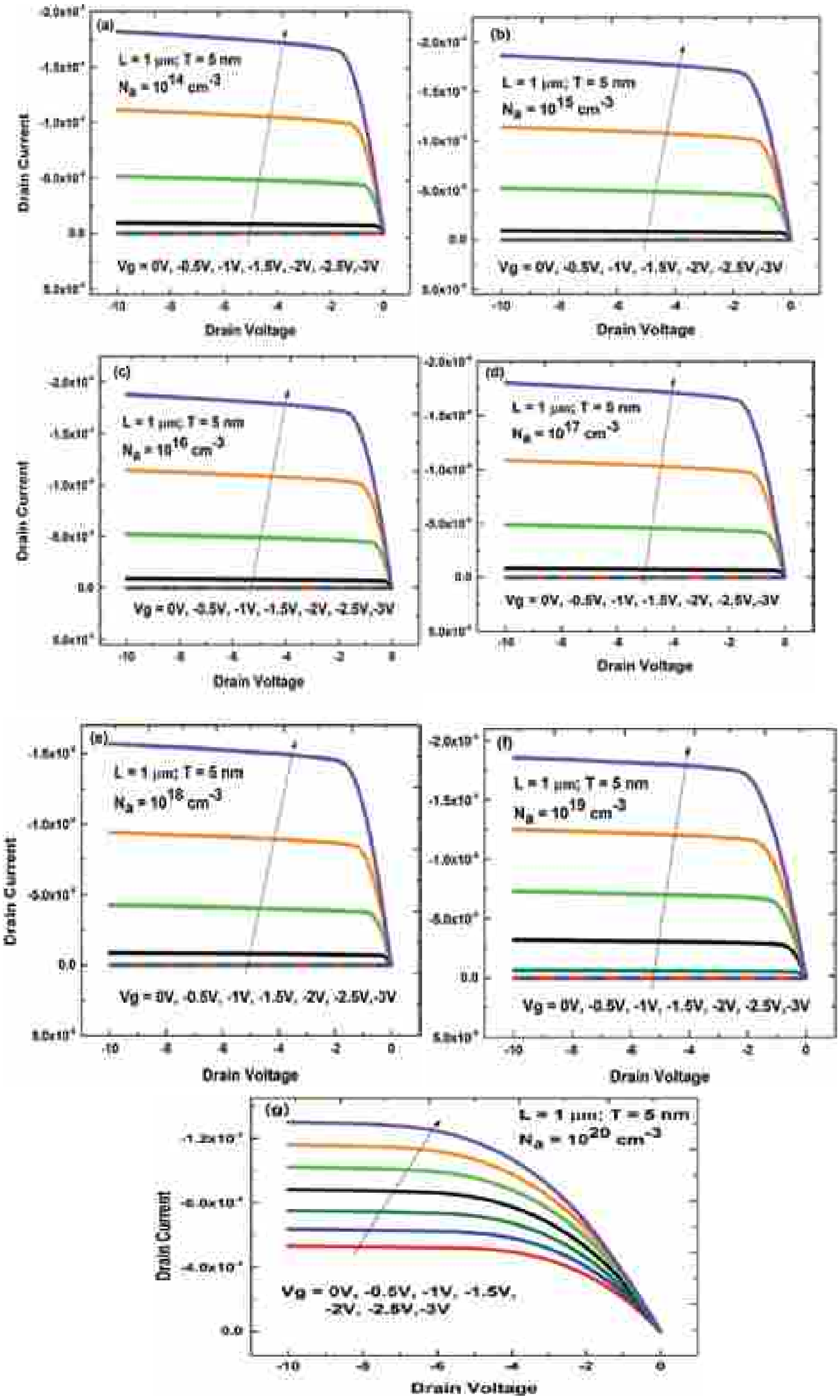


Figure B.6: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent $I_D$vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

APPENDIX C: DATA TABLES

Table C.1: Data table of accumulation mode Si-NW transistors with NW thickness of 100nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope(mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/µm)
100nm	10^{14}	0.5V	66.4696	-0.75	982	5.97e-5
		1V	66.7359	-0.225		
		1.5V	66.8154	0.28		
		2V	70.0670	0.8		
	10^{15}	0.5V	66.4696	-0.75	982	6.11e-5
		1V	66.7359	-0.225		
		1.5V	66.8154	0.28		
		2V	70.0670	0.8		
	10^{16}	0.5V	67.9219	-0.75	982	6.42e-5
		1V	66.79	-0.175		
		1.5V	66.9924	0.33		
		2V	67.9728	0.85		
	10^{17}	0.5V	777.33	-0.025	1500	9.23e-5
		1V	846.83	0.5		
		1.5V	854.8754	1		
		2V	845.5287	1.52		
	10^{18}	0.5V	5.9426e+003	Not measureable	3.9000e+003	0.000464
		1V	6.0962e+003	Not measureable		
		1.5V	6.1578e+003	Not measureable		
		2V	6.3397e+003	Not measureable		
	10^{19}	0.5V	Not measurable	Not measureable	Not measurable	0.00392
		1V	Not measurable	Not measureable		
		1.5V	Not measurable	Not measureable		
		2V	Not measurable	Not measureable		
	10^{20}	0.5V	Not measurable	Not measurable	Not measurable	0.0295
		1V	Not measurable	Not measureable		
		1.5V	Not measurable	Not measureable		
		2V	Not measurable	Not measureable		

Table C.2: Data table of accumulation mode Si-NW transistors with NW thickness of 75nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope(mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/µm)
75nm	10^{14}	0.5V	64.5	-0.75	1008	5.76e-5
		1V	64	-0.225		
		1.5V	64	0.275		
		2V	64.6	0.75		
	10^{15}	0.5V	64.5	-0.75	1008	5.89e-5
		1V	64	-0.225		
		1.5V	64	0.275		
		2V	64.6	0.75		
	10^{16}	0.5V	64.5	-0.72	1008	6.09e-5
		1V	64.8	-0.198		
		1.5V	65.1	0.299		
		2V	67.9	0.81		
	10^{17}	0.5V	69.3	-0.368	1058	7.85e-5
		1V	72	0.135		
		1.5V	71.7	0.652		
		2V	76.2	1.17		
	10^{18}	0.5V	4080	Not measurable	2713	0.000306
		1V	4130	Not measurable		
		1.5V	4180	Not measurable		
		2V	4250	Not measurable		
	10^{19}	0.5V	Not measurable	Not measurable	Not measurable	0.00276
		1V	Not measurable	Not measurable		
		1.5V	Not measurable	Not measurable		
		2V	Not measurable	Not measurable		
	10^{20}	0.5V	Not measurable	Not measurable	Not measurable	0.0219
		1V	Not measurable	Not measurable		
		1.5V	Not measurable	Not measurable		
		2V	Not measurable	Not measurable		

Table C.3: Data table of accumulation mode Si-NW transistors with NW thickness of 50nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL (mv/v)	Drive current (A/µm)
50nm	10^{14}	0.5V	64.0965	-0.75	982.2	5.49e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		
	10^{15}	0.5V	64.0965	-0.75	982.2	5.61e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		
	10^{16}	0.5V	64.0965	-0.75	982.2	5.73e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		
	10^{17}	0.5V	65.0554	-0.586	1008	6.59e-5
		1V	64.7202	-0.082		
		1.5V	63.2635	0.409		
		2V	65.3222	0.926		
	10^{18}	0.5V	2.3966e+003	Not measureable	1889.2	0.00018
		1V	2.3779e+003	Not measureable		
		1.5V	2.3140e+003	Not measureable		
		2V	476.9993	Not measureable		
	10^{19}	0.5V	1.6516e+004	Not measureable	Not measureable	0.00171
		1V	1.7553e+004	Not measureable		
		1.5V	1.8561e+004	Not measureable		
		2V	1.9208e+004	Not measureable		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	0.0141
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.4: Data table of accumulation mode Si-NW transistors with NW thickness of 25nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/µm)
25nm	10^{14}	0.5V	61.8	-0.762	1000	5.19e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		
	10^{15}	0.5V	61.8	-0.762	1000	5.3e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		
	10^{16}	0.5V	61.8	-0.762	1000	5.34e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		
	10^{17}	0.5V	63.3	-0.732	1000	5.45e-5
		1V	64.4	-0.225		
		1.5V	64.7	0.279		
		2V	64.6	0.779		
	10^{18}	0.5V	66	-0.184	1000	8.65e-5
		1V	69.1	0.323		
		1.5V	65.7	0.824		
		2V	69.7	1.33		
	10^{19}	0.5V	8.00E+03	Not measureable	Not measureable	0.000673
		1V	8.01E+03	Not measureable		
		1.5V	8.20E+03	Not measureable		
		2V	8.06E+03	Not measureable		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	0.00696
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.5: Data table of accumulation mode Si-NW transistors with NW thickness of 10nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/µm)
10nm	10^{14}	0.5V	61.8	-0.785	1000	4.97e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		
	10^{15}	0.5V	61.8	-0.785	1000	5.07e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		
	10^{16}	0.5V	61.8	-0.785	1000	5.07e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		
	10^{17}	0.5V	61.8	-0.785	1000	4.83e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.22		
		2V	62.2	0.73		
	10^{18}	0.5V	64.9	-0.66	1015.4	4.97e-5
		1V	65.2	-0.195		
		1.5V	64.2	0.345		
		2V	64.2	0.842		
	10^{19}	0.5V	98.6	0.8	1703.4	1.60e-4
		1V	120	1.31		
		1.5V	117	1.78		
		2V	125	2.32		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	2.45e-3
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.6: Data table of accumulation mode Si-NW transistors with NW thickness of 5nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL (mv/v)	Drive current (A/µm)
5nm	10^{14}	0.5V	61.15	-0.825	1000	4.82e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{15}	0.5V	61.15	-0.825	1000	4.91e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{16}	0.5V	61.15	-0.825	1000	4.9e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{17}	0.5V	61.15	-0.825	1000	4.58e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{18}	0.5V	61.92	-0.81	1022	4.04e-5
		1V	65.77	-0.275		
		1.5V	65.79	0.225		
		2V	64.49	0.725		
	10^{19}	0.5V	65.6	-0.25	1000	7.02e-5
		1V	67.33	0.25		
		1.5V	67.85	0.75		
		2V	67.48	1.25		
	10^{20}	0.5V	7552.3	Not measureable	4440	0.000954
		1V	7786.1	Not measureable		
		1.5V	8112.2	Not measureable		
		2V	8717.1	Not measureable		

DATASET USED FOR COMPARATIVE ASSESSMENT OF SINGLE CRYSTAL AND POLYCRYSTALLINE SILICON NANOWIRE BIOSENSORS

APPENDIX D: SINGLE CRYSTAL SILICON NANOWIRE

1. 1e16/cm^3

NW thickness 10nm:

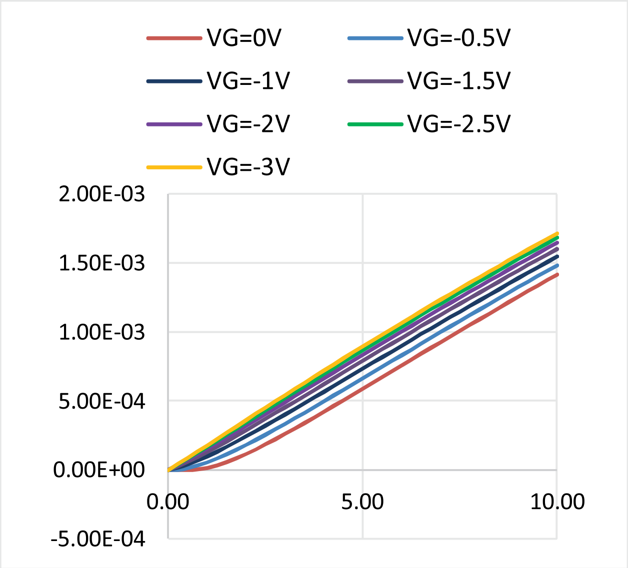


Fig.01: Ids vs Vds curves

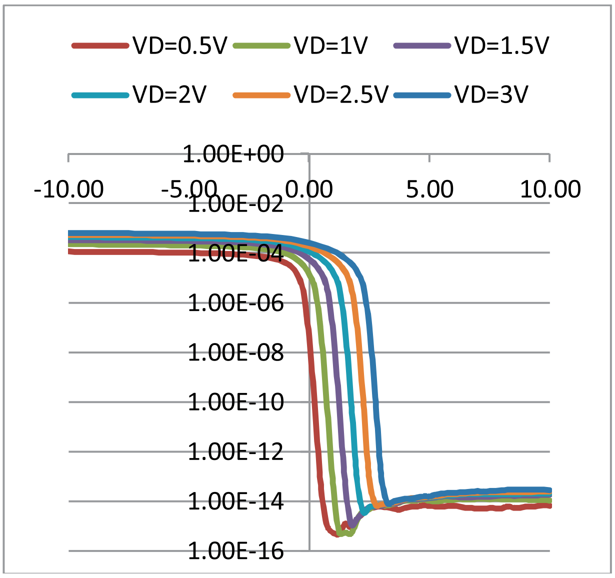


Fig.02: Ids vs Vgs curves

NW thickness 25nm:

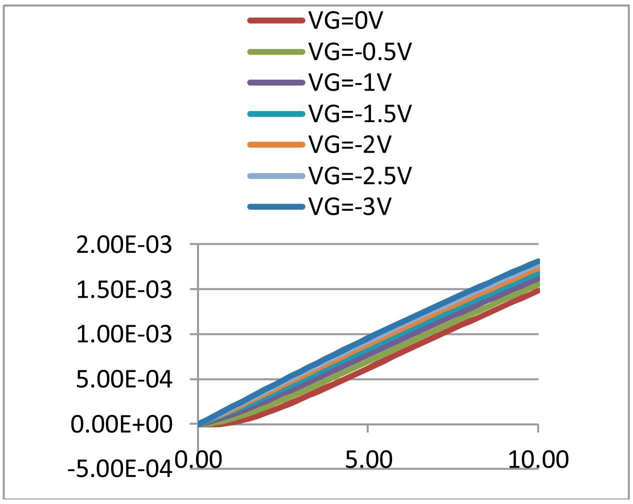


Fig.03: Ids vs Vds curves

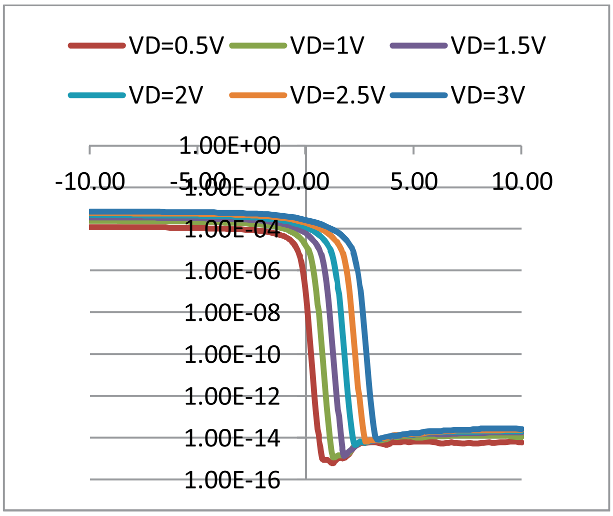


Fig.04: Ids vs Vgs curves

NW thickness 50nm:

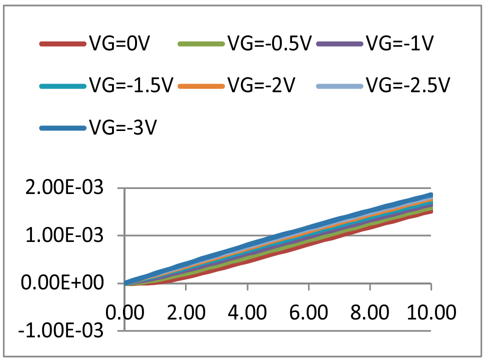


Fig.06: Ids vs Vgs curves

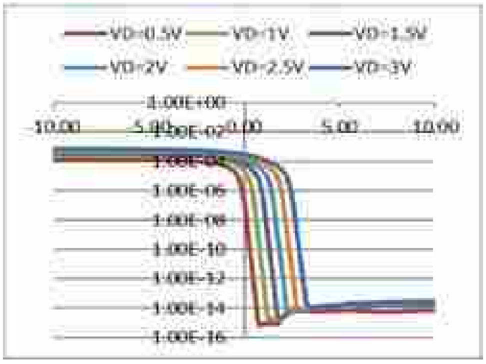


Fig.05: Ids vs Vds curves

NW thickness 75nm:

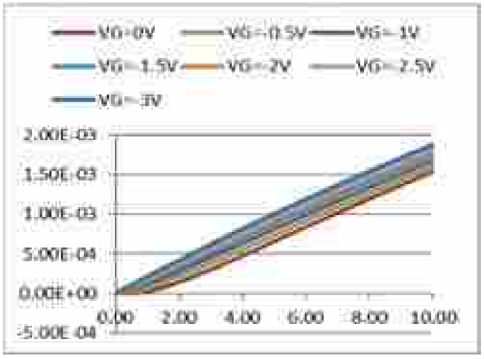


Fig.07: Ids vs Vds curves

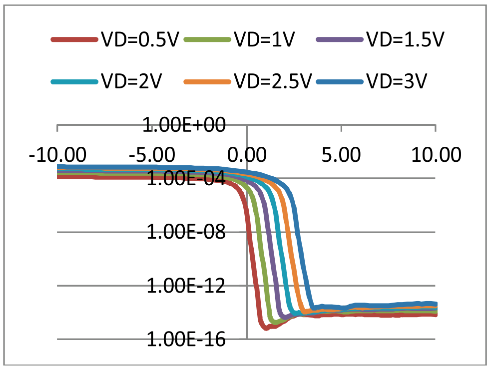


Fig.08: Ids vs Vgs curves

NW thickness 100nm:

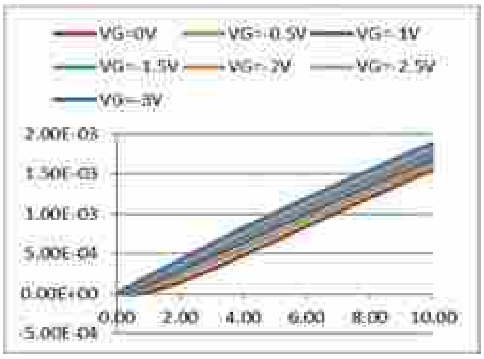


Fig.09: Ids vs Vds curves

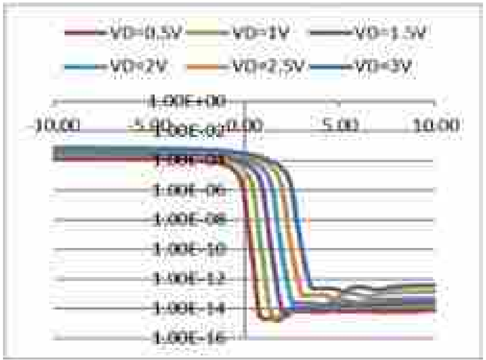


Fig.10: Ids vs Vgs curves

2. 2e16/cm^3

NW thickness 10nm:

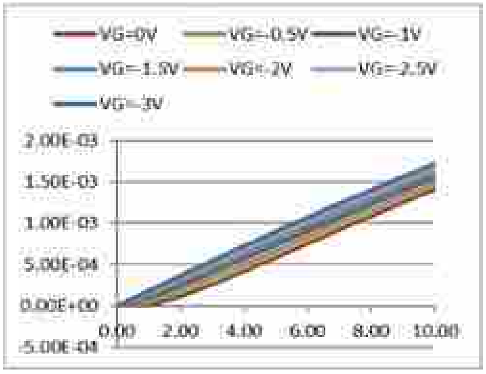


Fig.11: Ids vs Vds curves

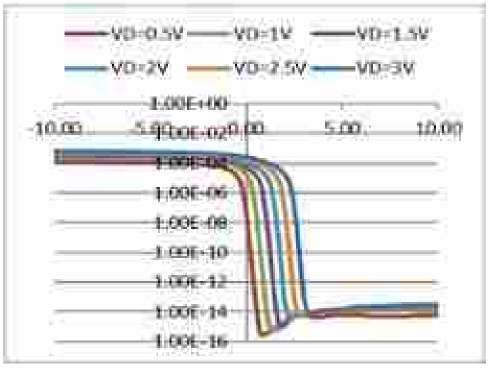


Fig.12: Ids vs Vgs curves

NW thickness 25nm:

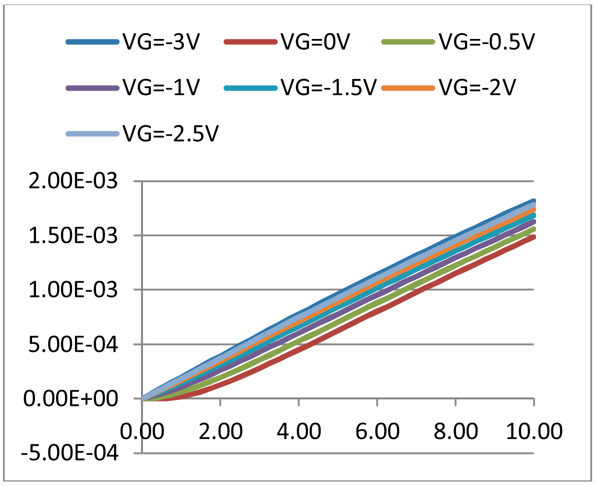


Fig.13: Ids vs Vds curves

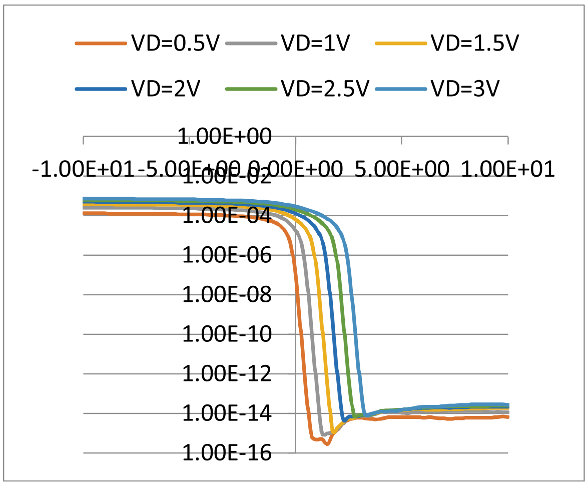


Fig.14: Ids vs Vgs curves

NW thickness 50nm:

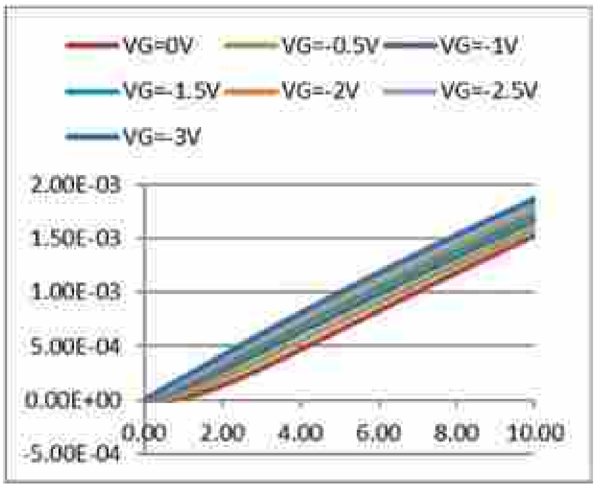


Fig.15: Ids vs Vds curves

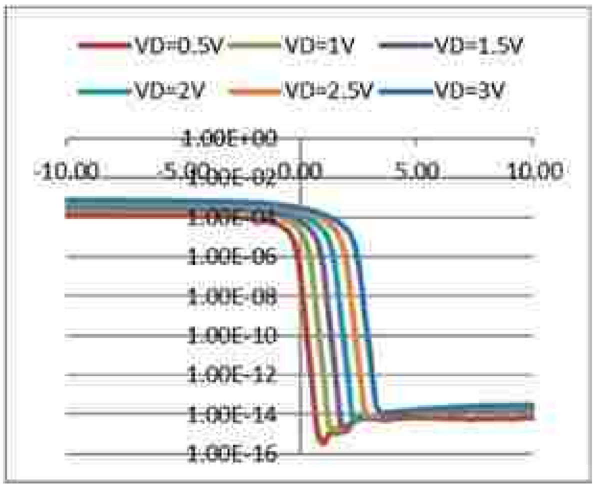


Fig.16: Ids vs Vgs curves

NW thickness 75nm:

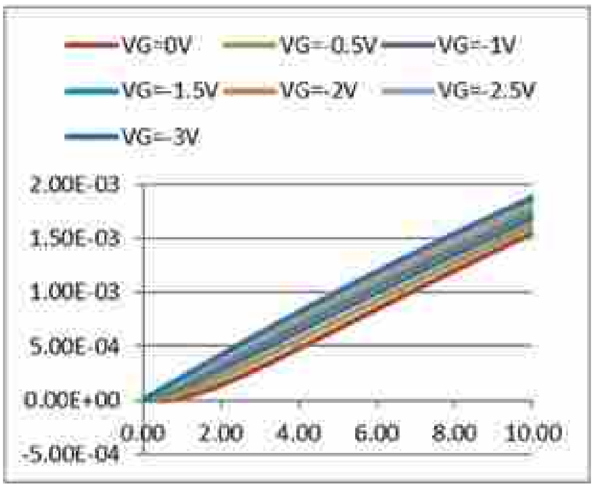


Fig.17: Ids vs Vds curves

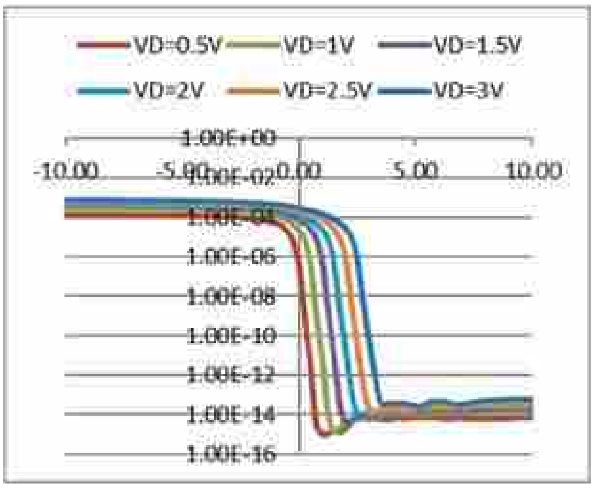
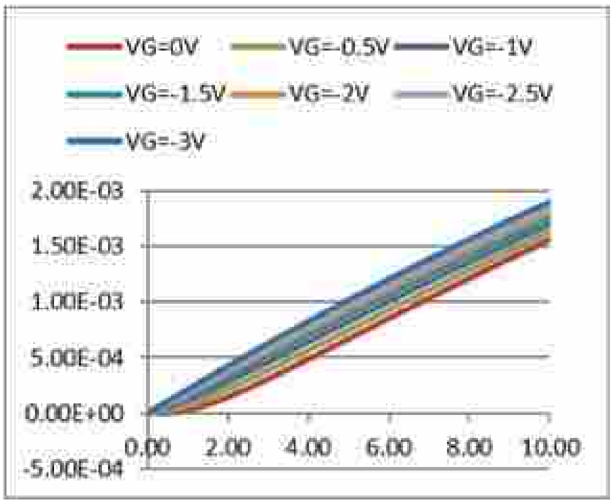


Fig.18: Ids vs Vgs curves

NW thickness 100nm:



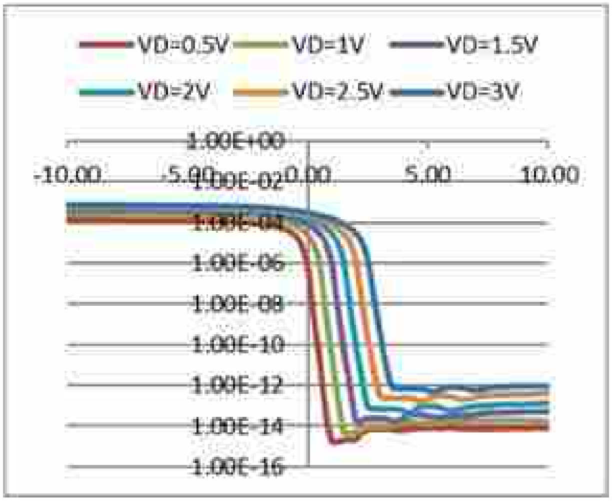
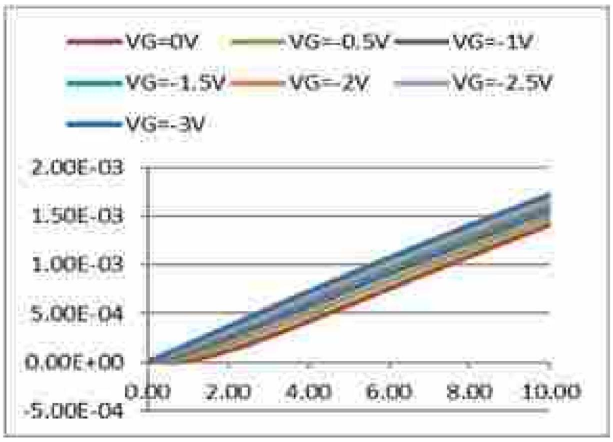


Fig.19: Ids vs Vds curves

Fig.20: Ids vs Vgs curves

3. 4e16/cm^3

NW thickness 10nm:



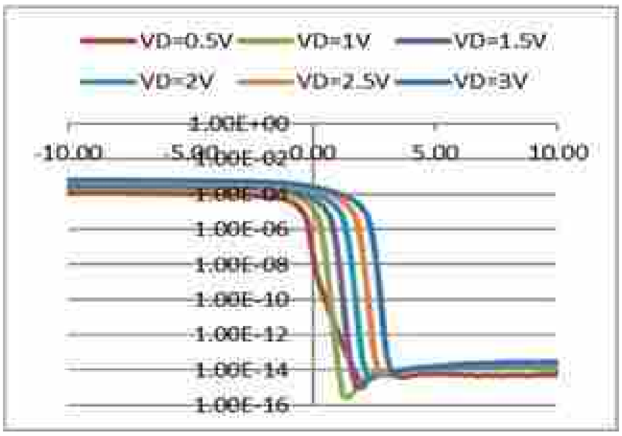
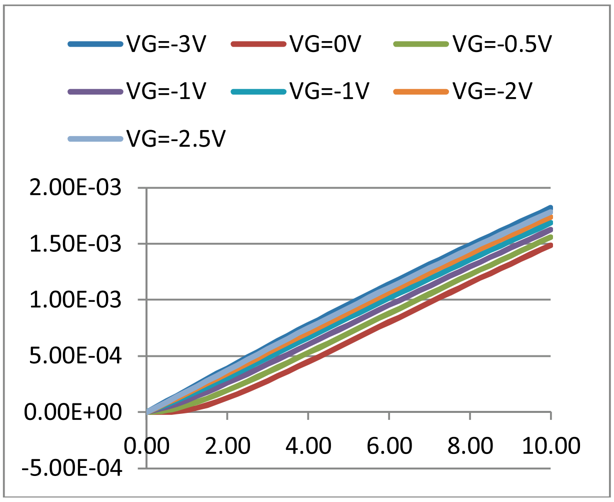


Fig.21: Ids vs Vds curves

Fig.22: Ids vs Vgs curves

NW thickness 25nm:



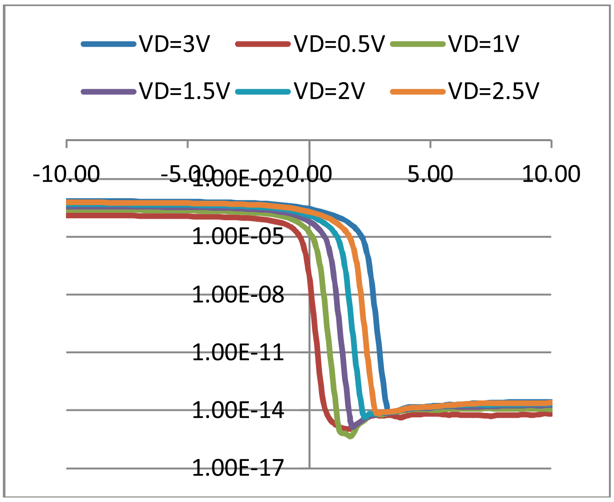


Fig.23: Ids vs Vds curves

Fig.24: Ids vs Vgs curves

NW thickness 50nm:

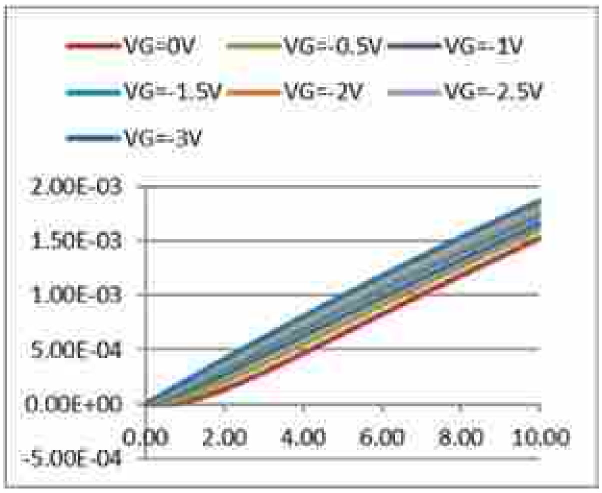


Fig.25: Ids vs Vds curves

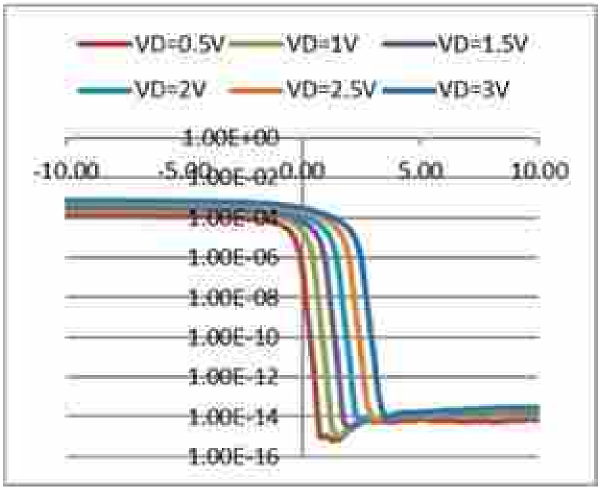


Fig.26: Ids vs Vgs curves

NW thickness 75nm:

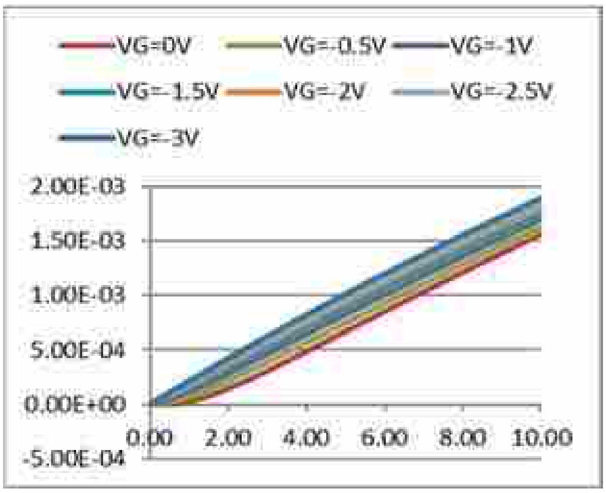


Fig.27: Ids vs Vds curves

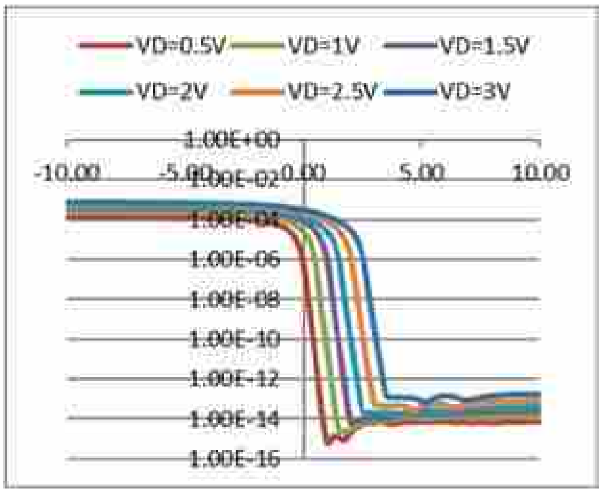


Fig.28: Ids vs Vgs curves

NW thickness 100nm:

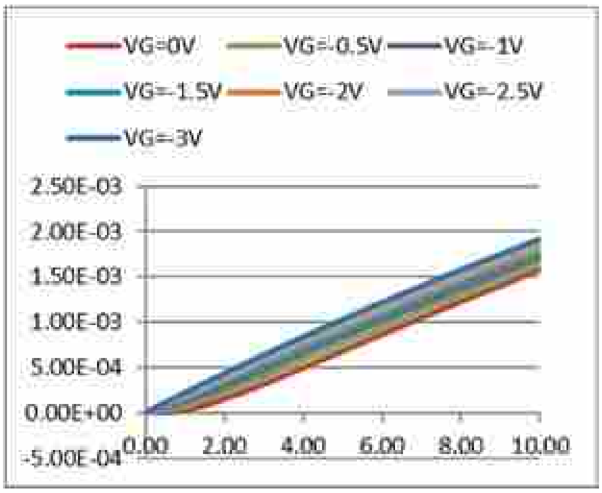


Fig.29: Ids vs Vds curves

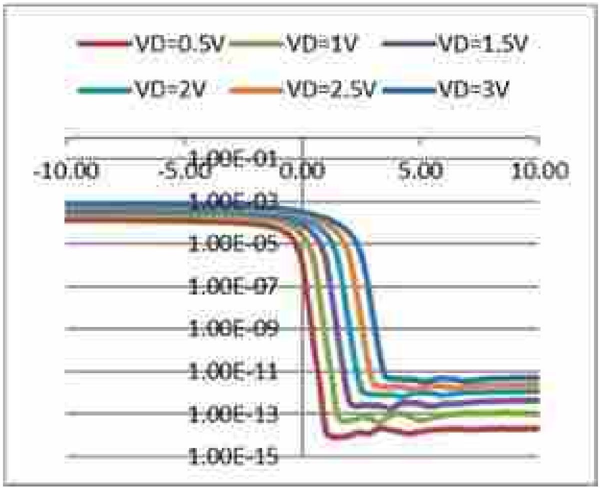


Fig.30: Ids vs Vgs curves

4. 6e16/cm^3

NW thickness 10nm:

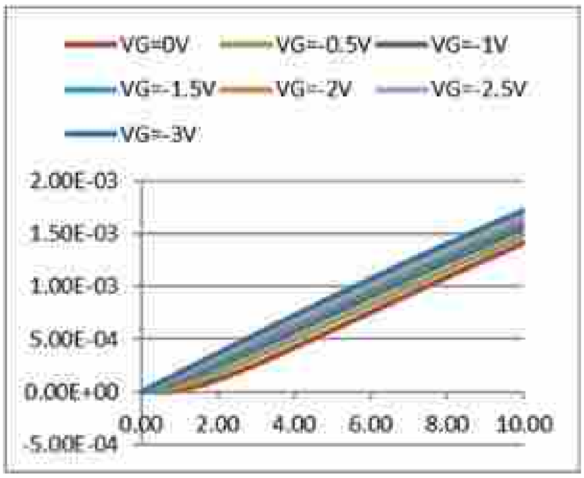


Fig.31: Ids vs Vds curves

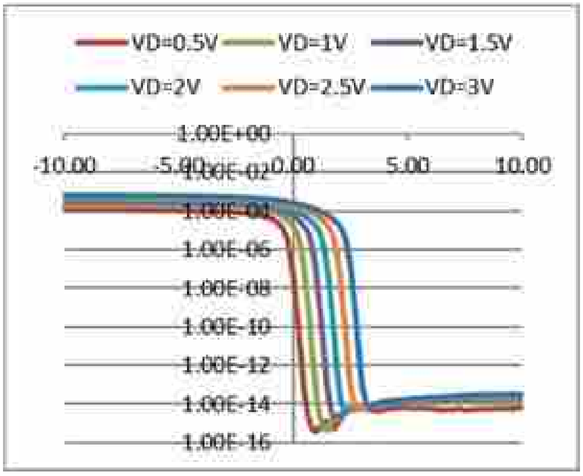


Fig.32: Ids vs Vgs curves

NW thickness 25nm:

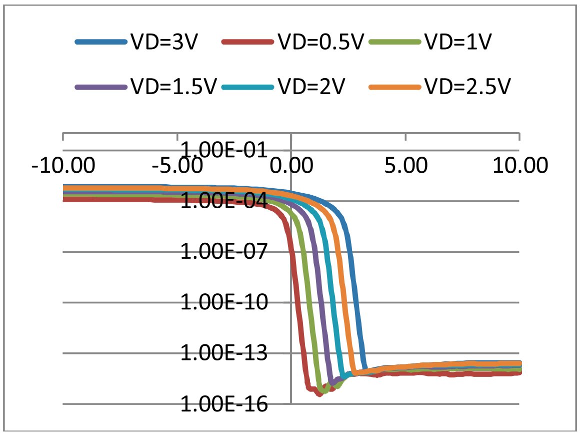


Fig.33: Ids vs Vds curves

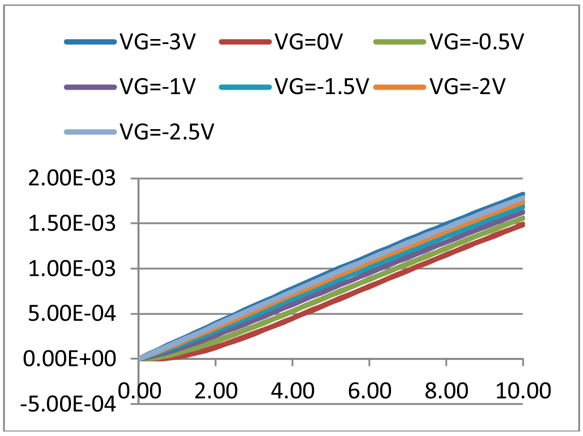


Fig.34: Ids vs Vgs curves

NW thickness 50nm:

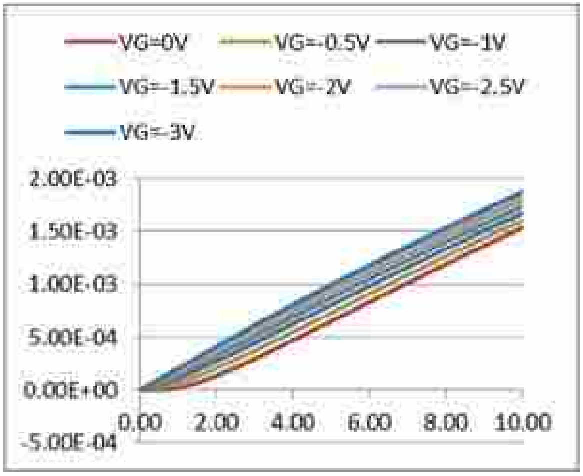


Fig.35: Ids vs Vds curves

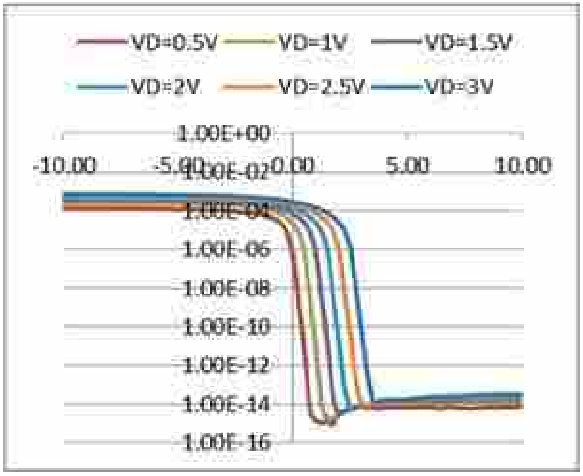


Fig.36: Ids vs Vgs curves

NW thickness 75nm:

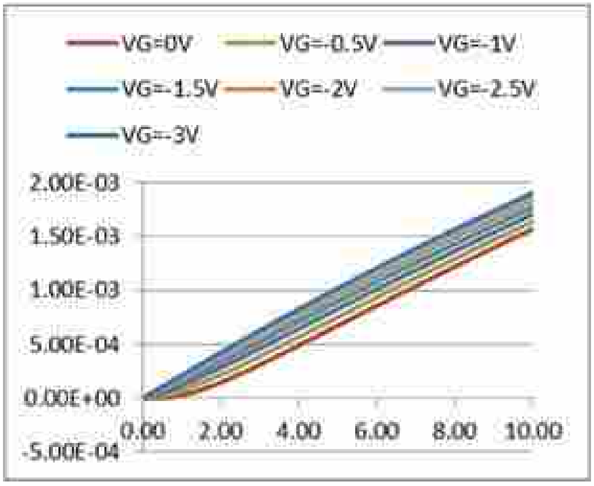


Fig.37: Ids vs Vds curves

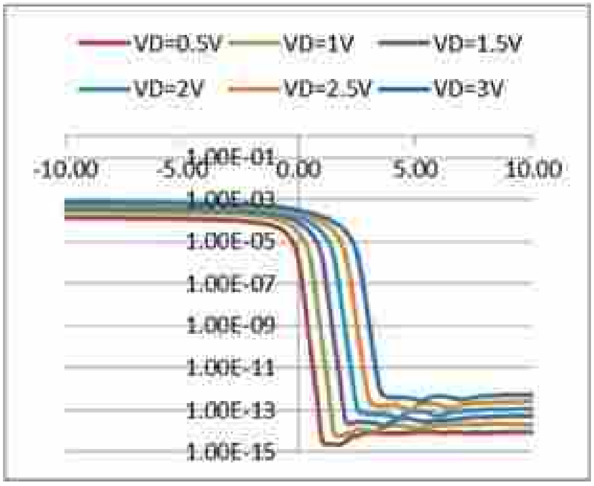


Fig.38: Ids vs Vgs curves

NW thickness 100nm:

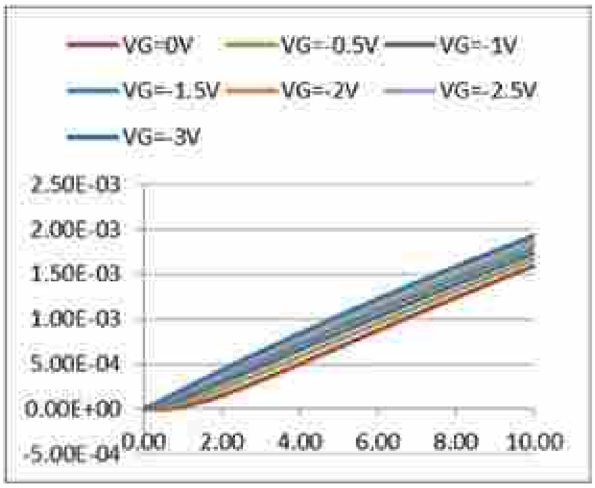


Fig.39: Ids vs Vds curves

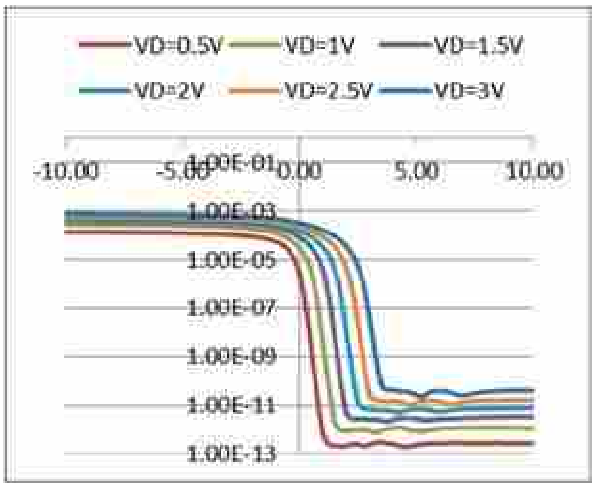


Fig.40: Ids vs Vgs curves

5. **8e16/cm^3**

NW thickness 10nm:

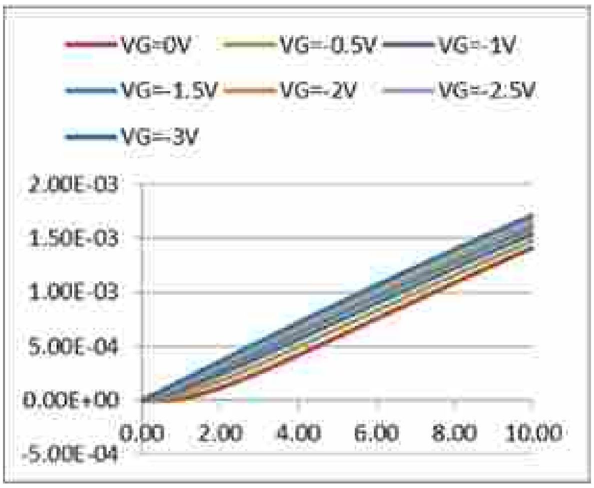


Fig.41: Ids vs Vds curves

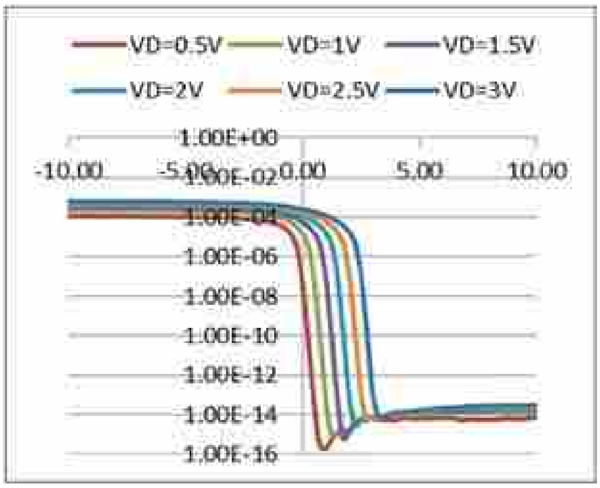


Fig.42: Ids vs Vgs curves

NW thickness 25nm:

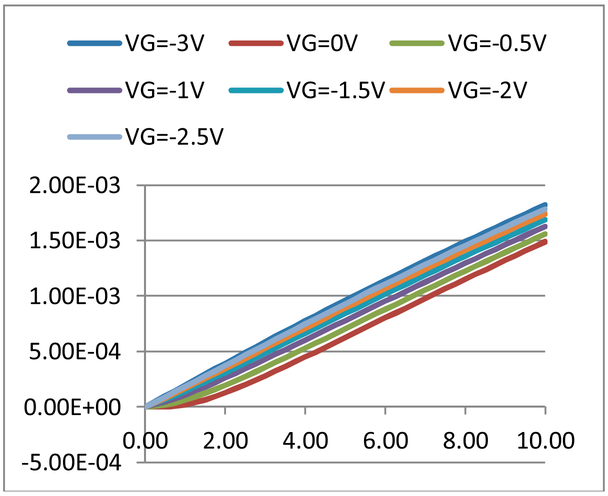


Fig.43: Ids vs Vds curves

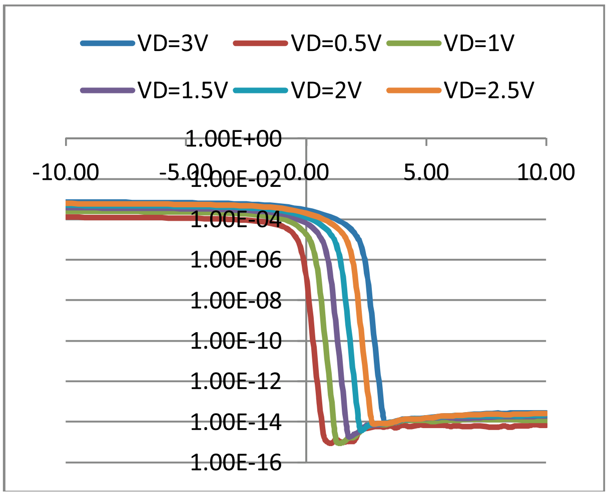


Fig.44: Ids vs Vgs curves

NW thickness 50nm:

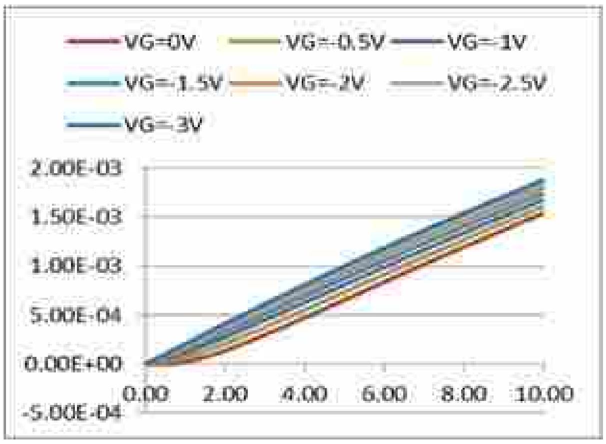


Fig.45: Ids vs Vds curves

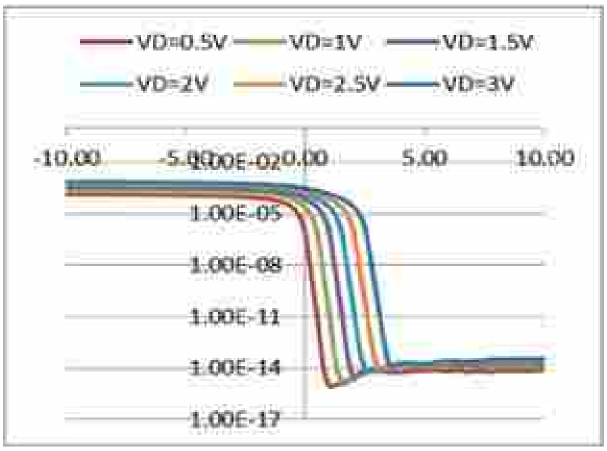


Fig.46: Ids vs Vgs curves

NW thickness 75nm:

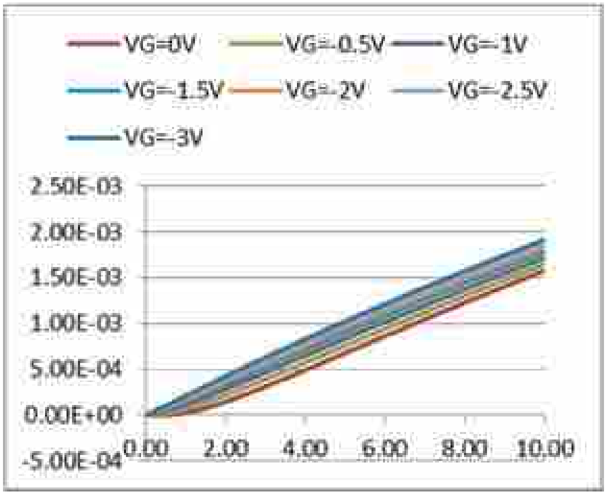


Fig.47: Ids vs Vds curves

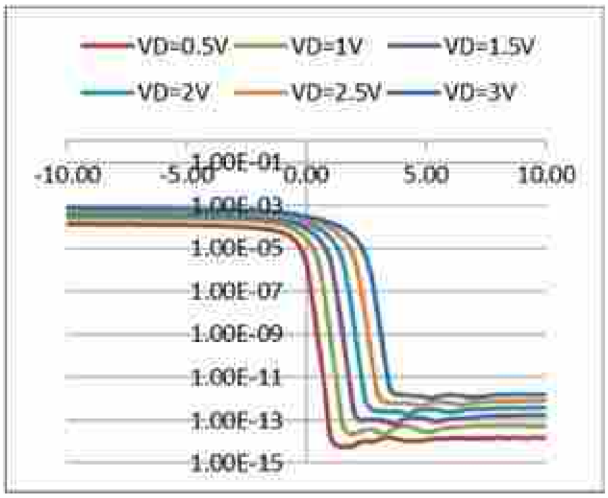


Fig.48: Ids vs Vgs curves

NW thickness 100nm:

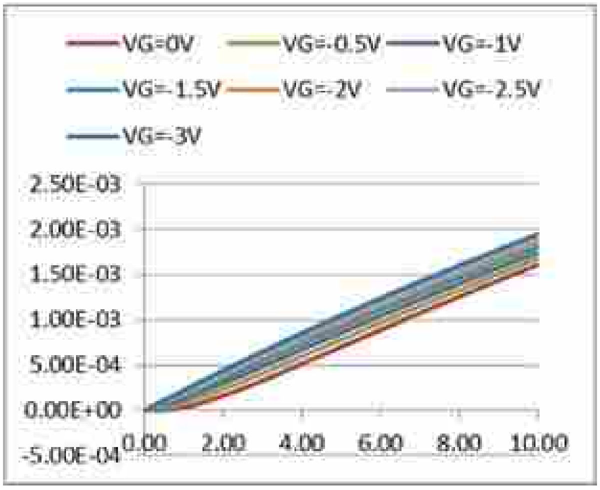


Fig.49: Ids vs Vds curves

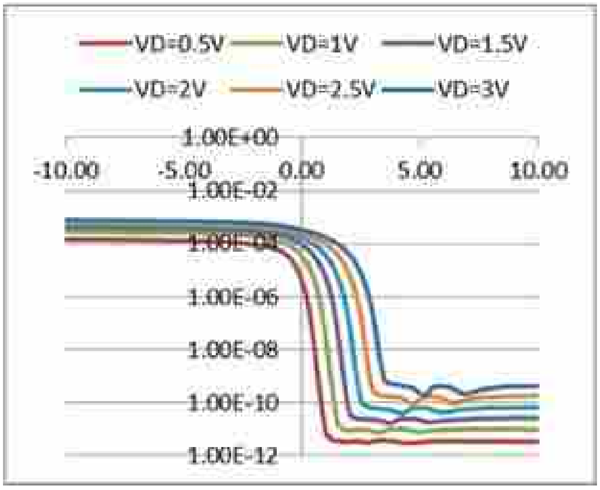


Fig.50: Ids vs Vgs curves

6. 1e17/cm^3

NW thickness 10nm:

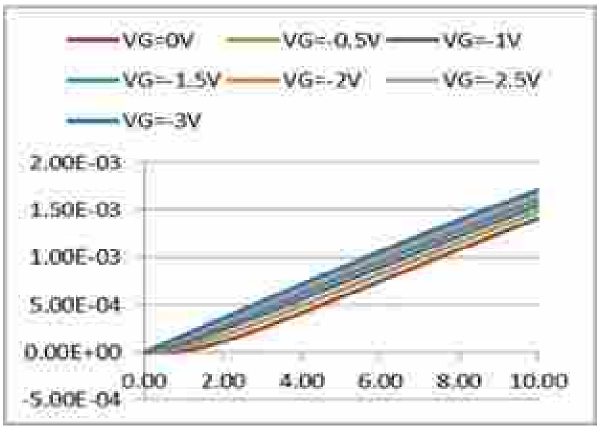


Fig.51: Ids vs Vds curves

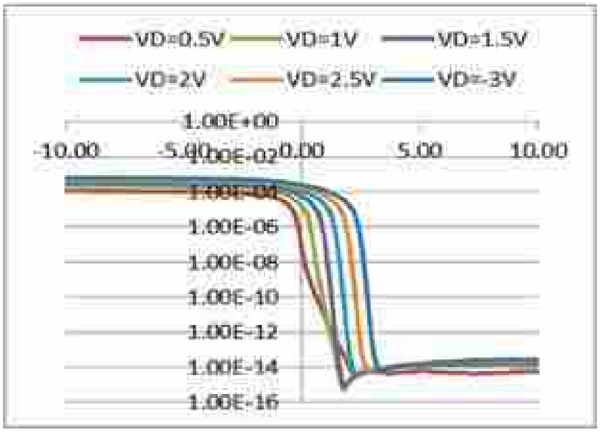


Fig.52: Ids vs Vgs curves

NW thickness 25nm:

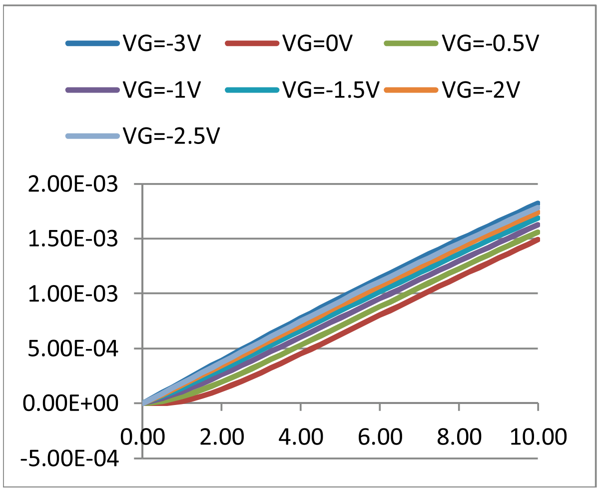


Fig.53: Ids vs Vds curves

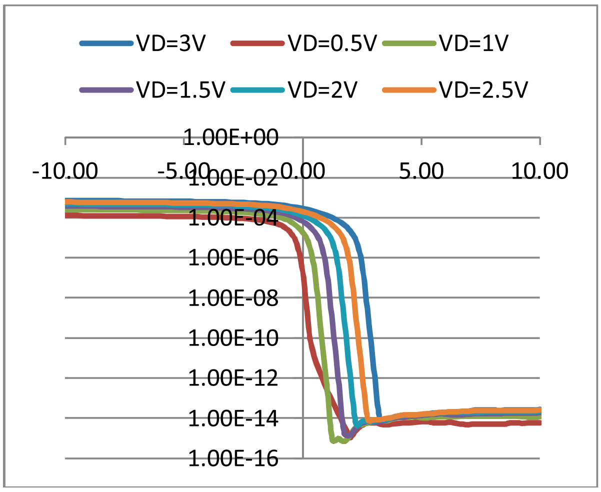


Fig.54: Ids vs Vgs curves

NW thickness 50nm:

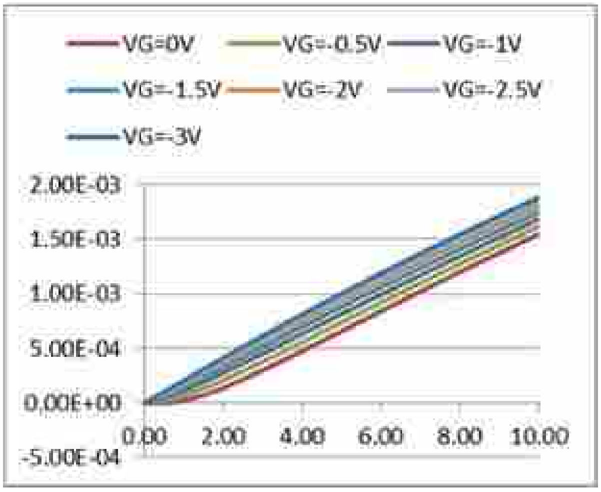


Fig.55: Ids vs Vds curves

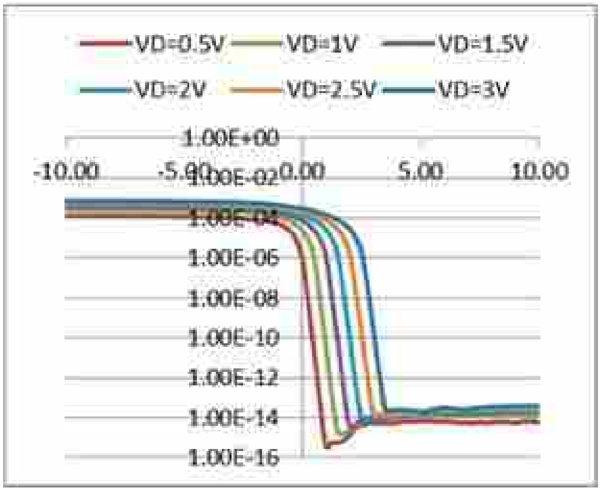


Fig.56: Ids vs Vgs curves

NW thickness 75nm:

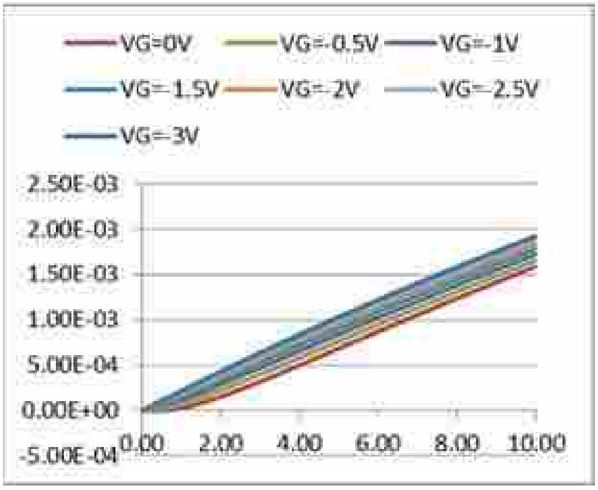


Fig.57: Ids vs Vds curves

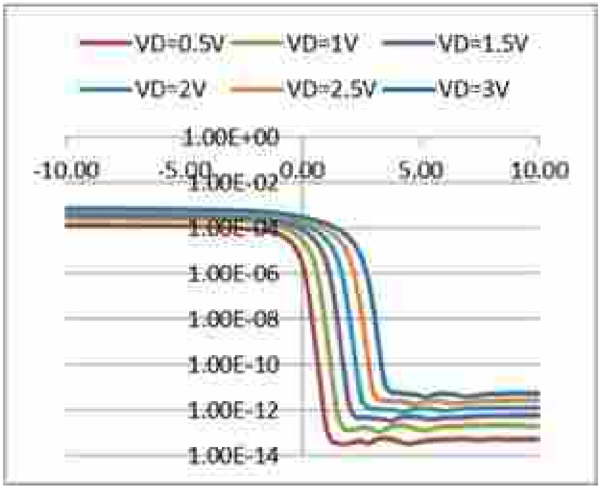


Fig.58: Ids vs Vgs curves

NW thickness 100nm:

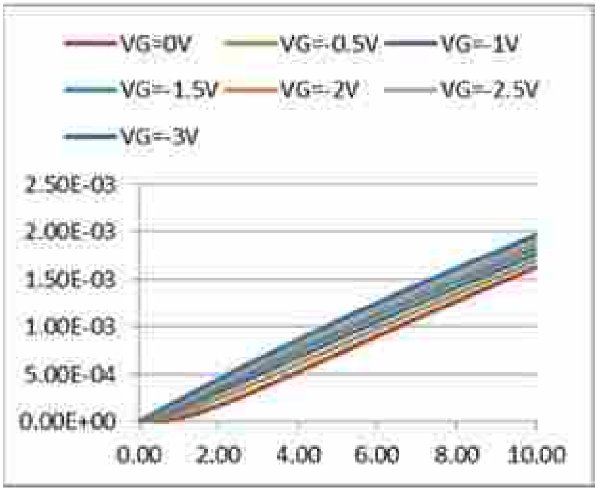


Fig.59: Ids vs Vds curves

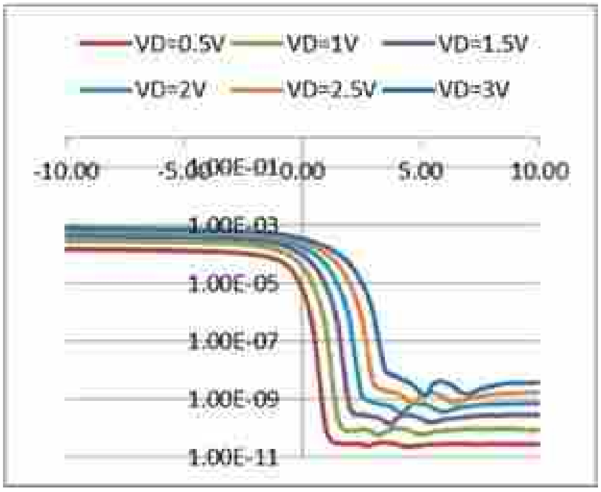


Fig.60: Ids vs Vgs curves

7. 2e17/cm^3

NW thickness 10nm:

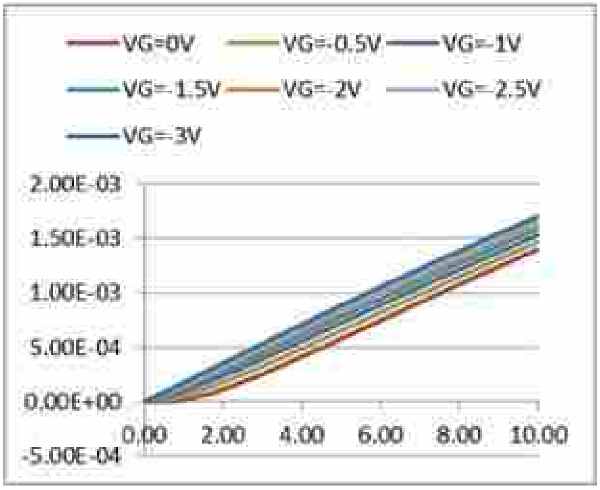


Fig.61: Ids vs Vds curves

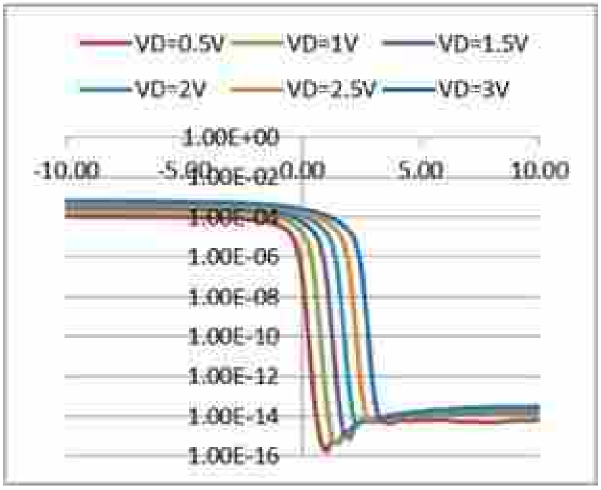


Fig.62: Ids vs Vgs curves

NW thickness 25nm:

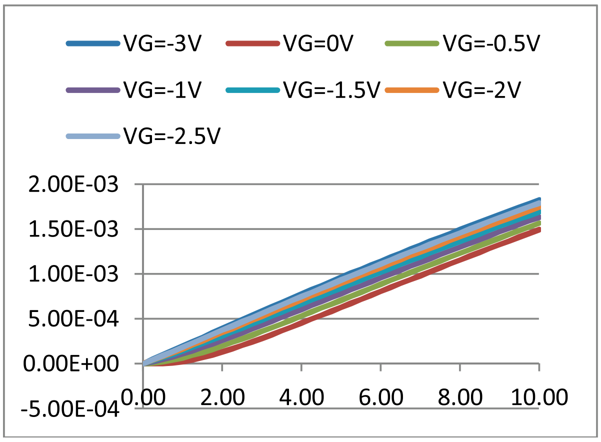


Fig.63: Ids vs Vds curves

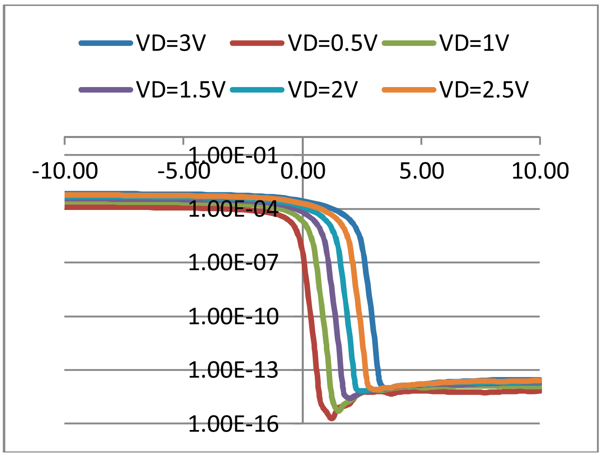


Fig.64: Ids vs Vgs curves

NW thickness 50nm:

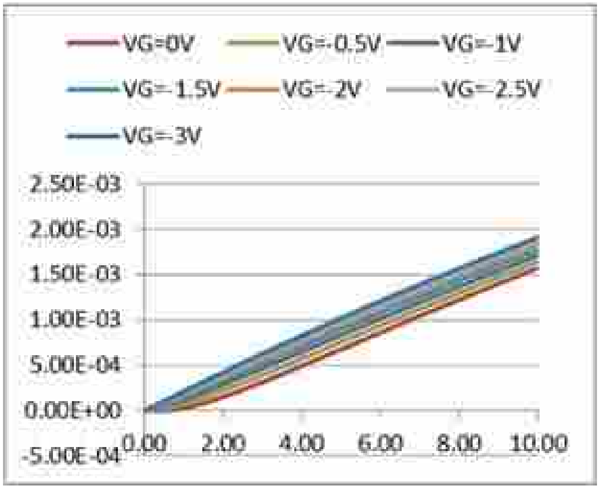


Fig.65: Ids vs Vds curves

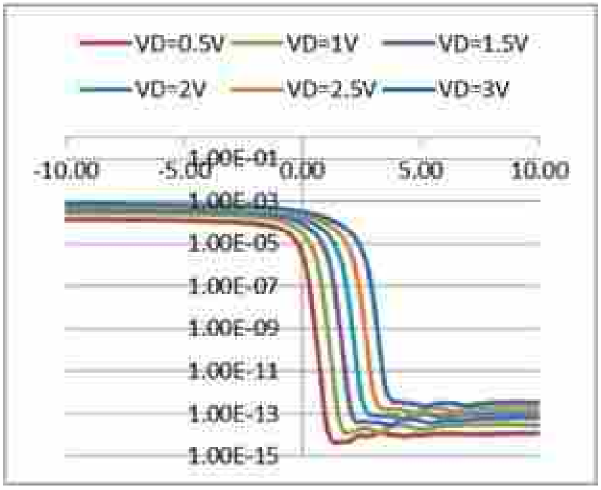


Fig.66: Ids vs Vgs curves

NW thickness 75nm:

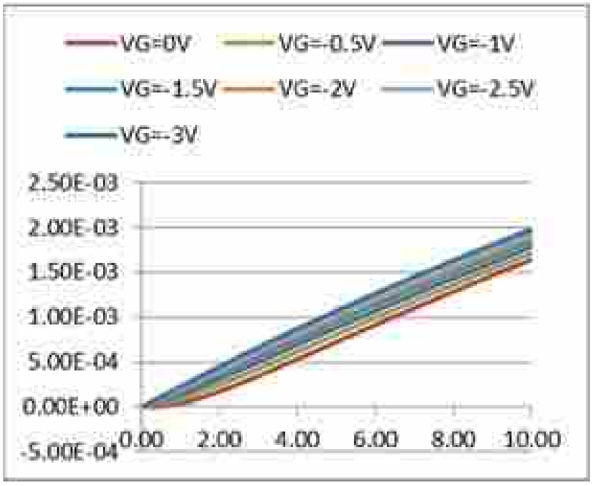


Fig.67: Ids vs Vds curves

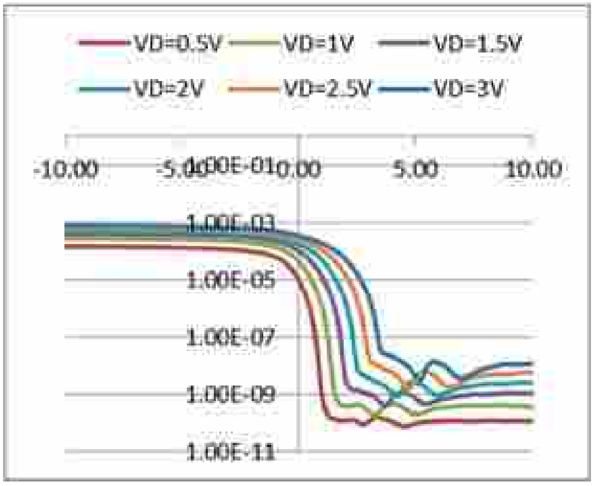


Fig.68: Ids vs Vgs curves

NW thickness 100nm:

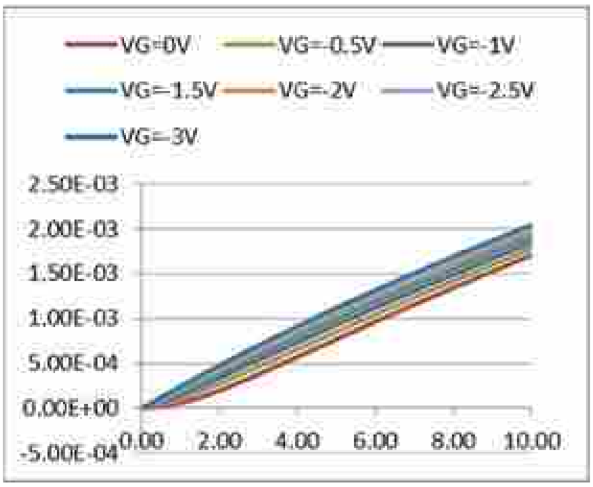


Fig.69: Ids vs Vds curves

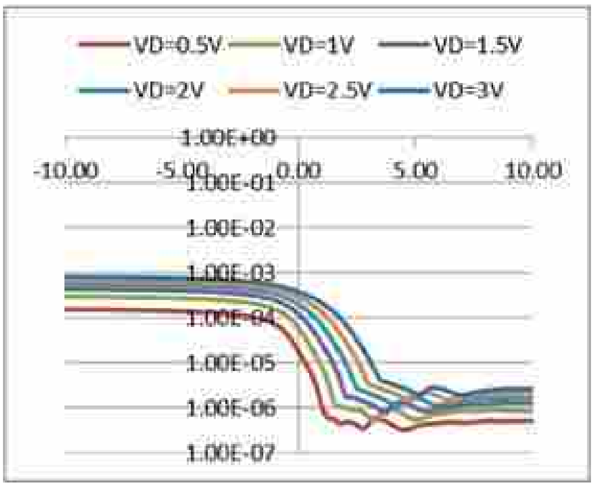


Fig.70: Ids vs Vgs curves

8. 4e17/cm^3

NW thickness 10nm:

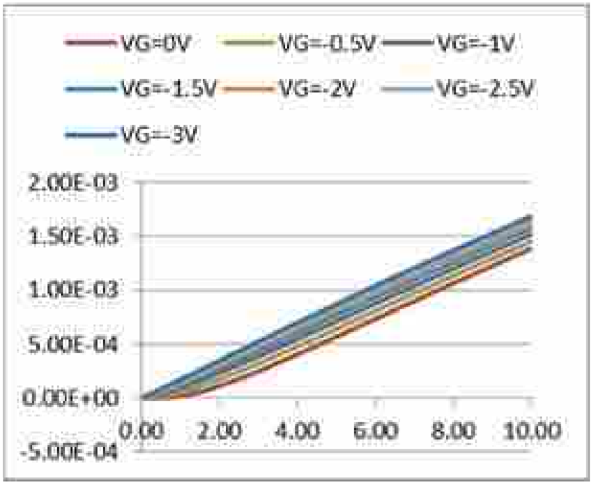


Fig.71: Ids vs Vds curves

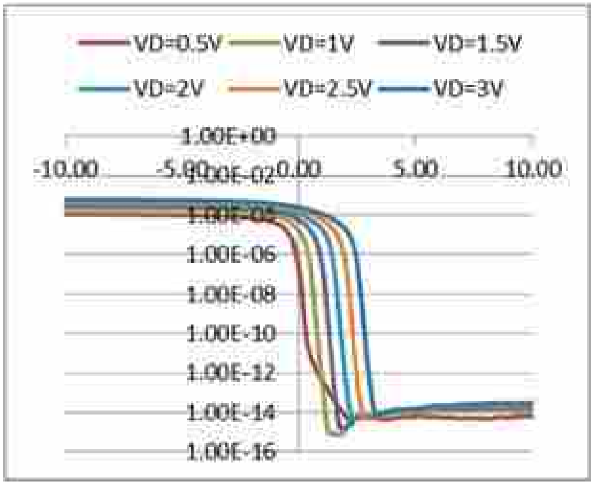


Fig.72: Ids vs Vgs curves

NW thickness 25nm:

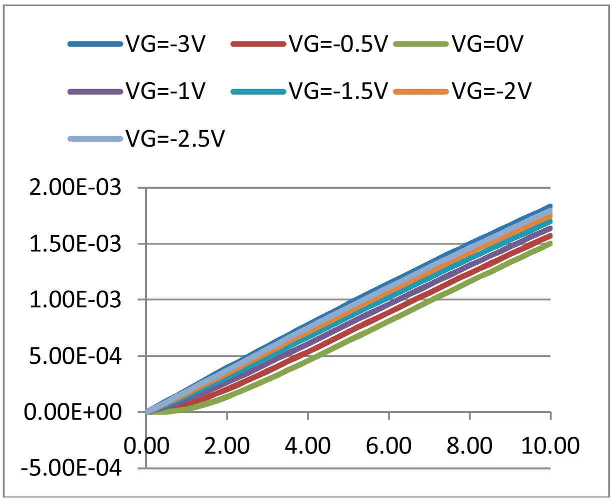


Fig.73: Ids vs Vds curves

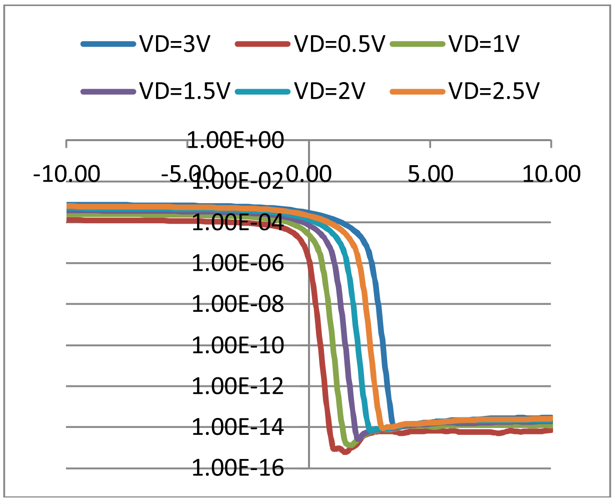


Fig.74: Ids vs Vgs curves

NW thickness 50nm:

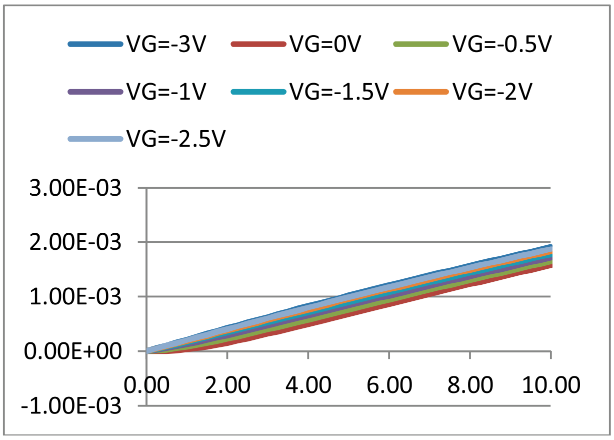


Fig.75: Ids vs Vds curves

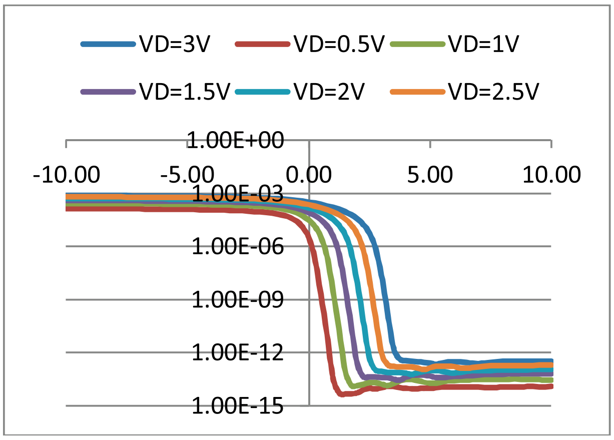


Fig.76: Ids vs Vgs curves

NW thickness 50nm:

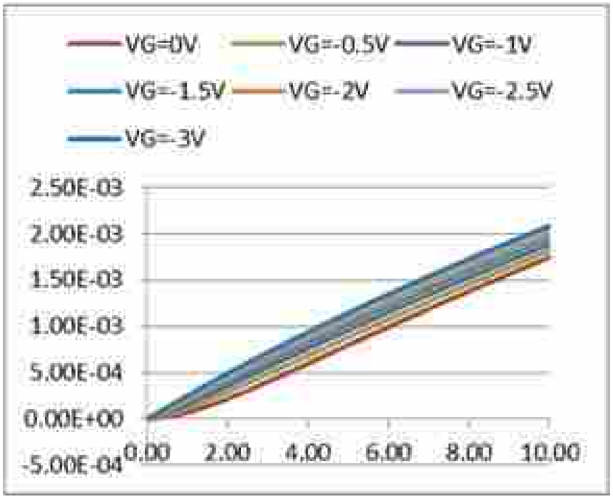


Fig.77: Ids vs Vds curves

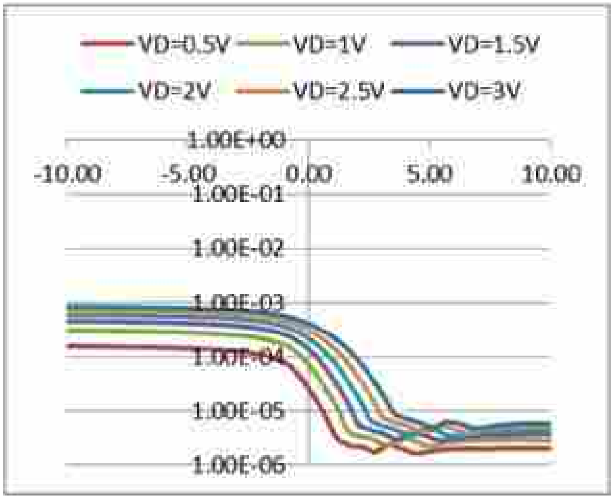


Fig.78: Ids vs Vgs curves

NW thickness 100nm

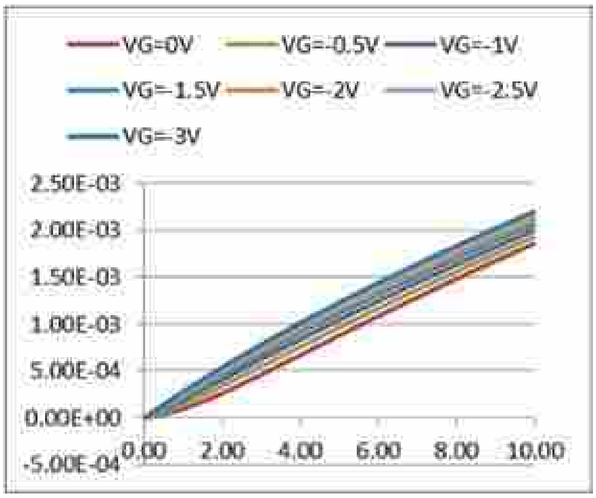


Fig.79: Ids vs Vds curves

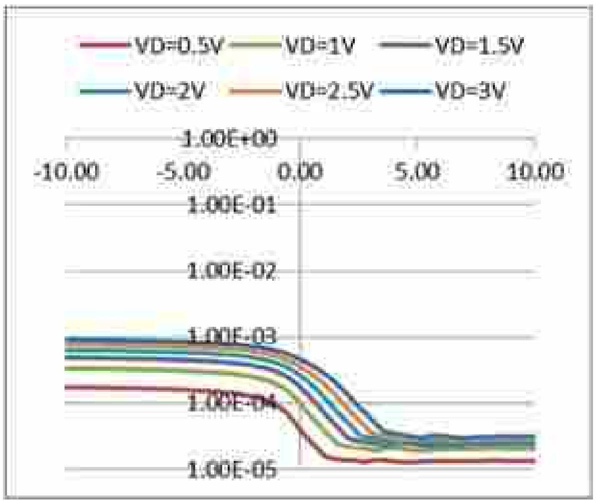


Fig.80: Ids vs Vgs curves

9. 6e17/cm^3

NW thickness 10nm:

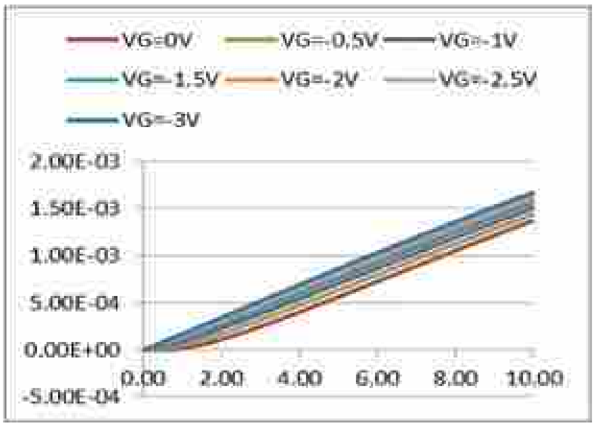


Fig.81: Ids vs Vds curves

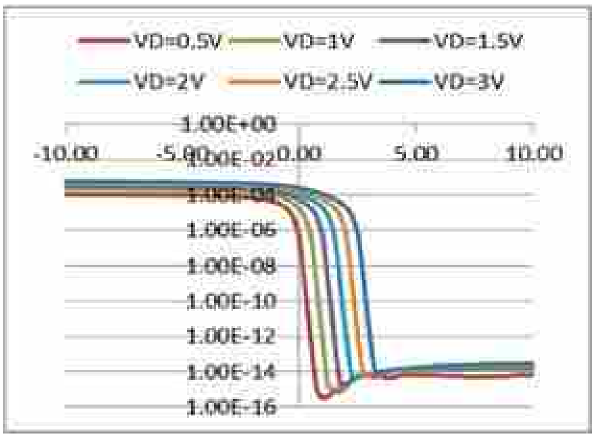


Fig.82: Ids vs Vgs curves

NW thickness 25nm:

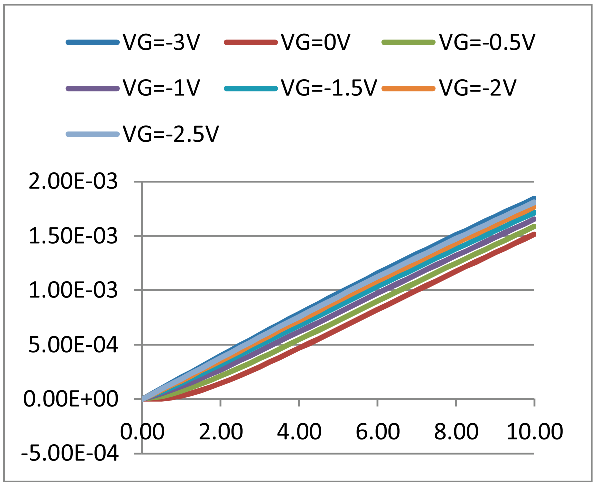


Fig.83: Ids vs Vds curves

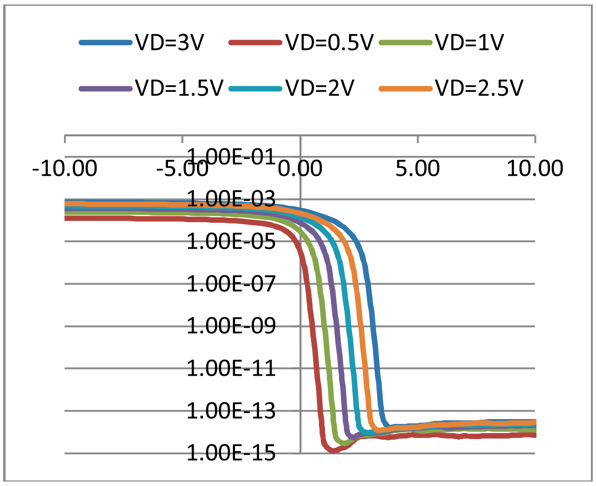


Fig.84: Ids vs Vgs curves

NW thickness 50nm:

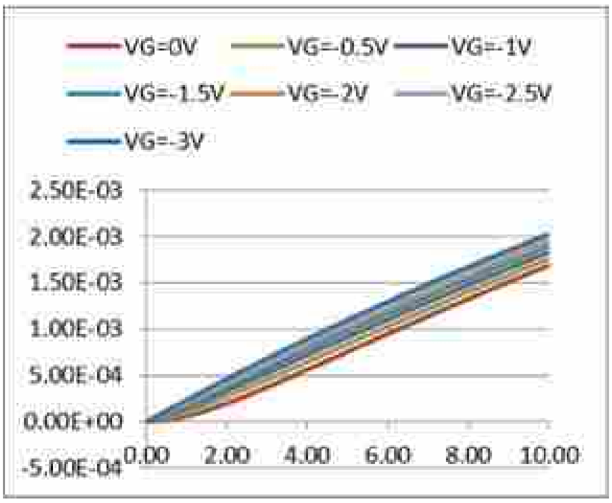


Fig.85: Ids vs Vds curves

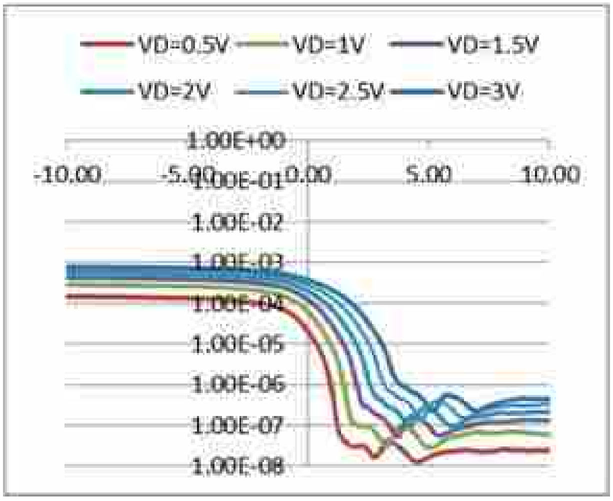


Fig.86: Ids vs Vgs curves

NW thickness 75nm:

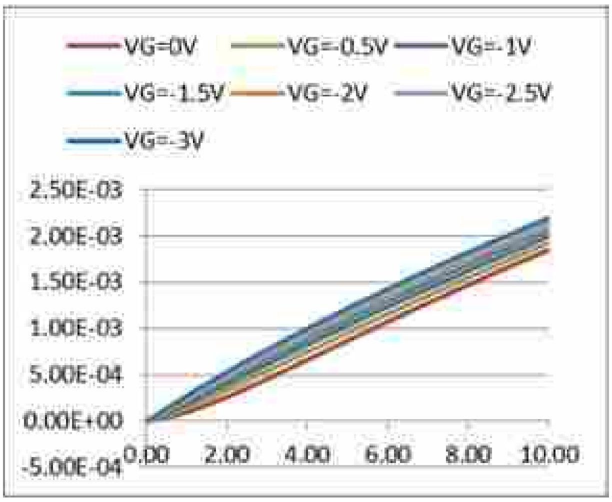


Fig.87: Ids vs Vds curves

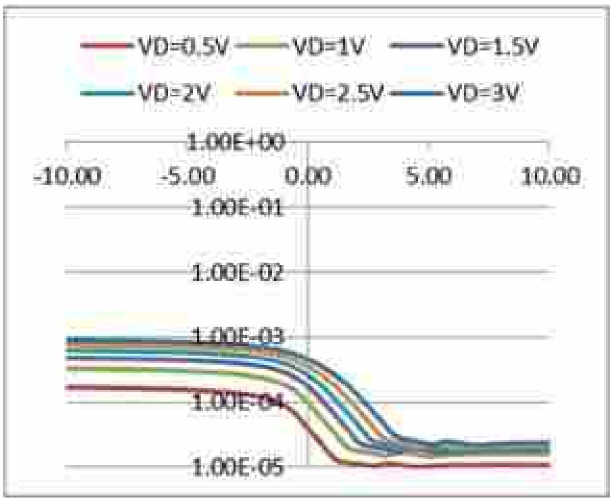


Fig.88: Ids vs Vgs curves

NW thickness 100nm:

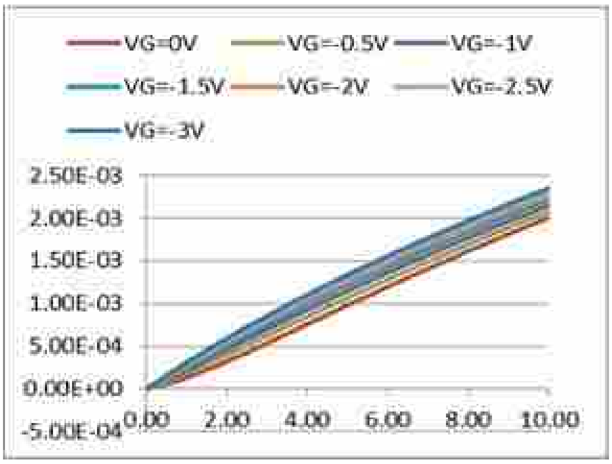


Fig.89: Ids vs Vds curves

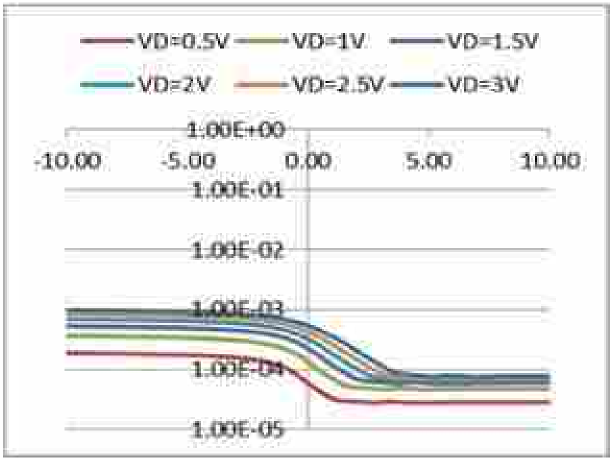


Fig.90: Ids vs Vgs curves

10. 8e17/cm^3

NW thickness 10nm:

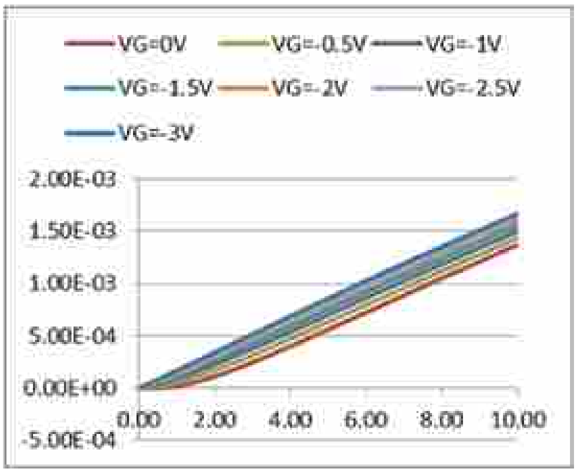


Fig.91: Ids vs Vds curves

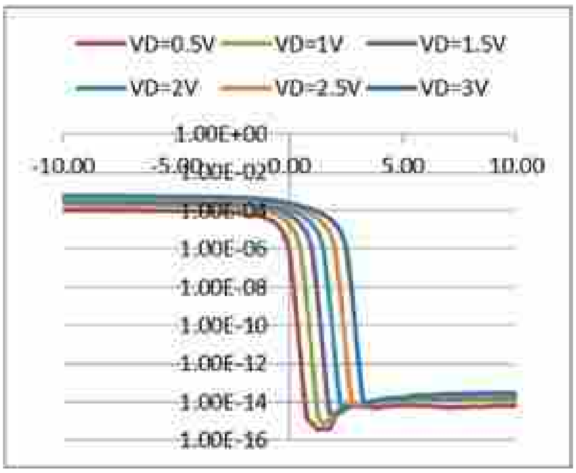


Fig.92: Ids vs Vgs curves

NW thickness 25nm:

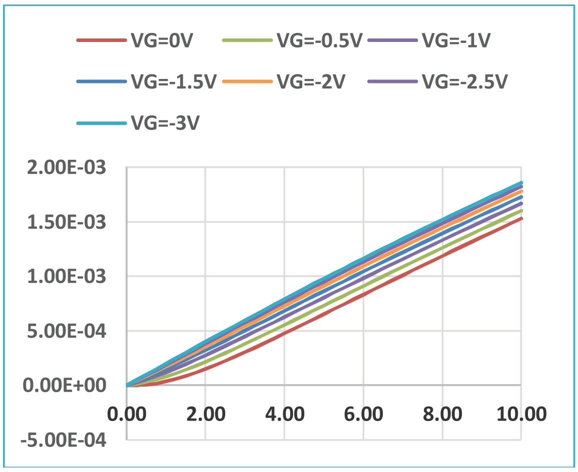


Fig.93: Ids vs Vds curves

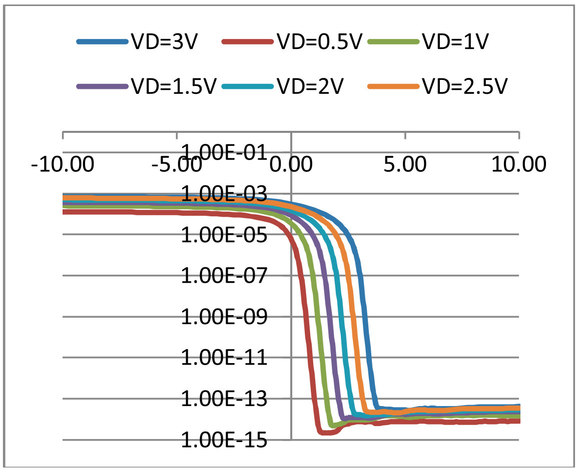


Fig.94: Ids vs Vgs curves

NW thickness 50nm:

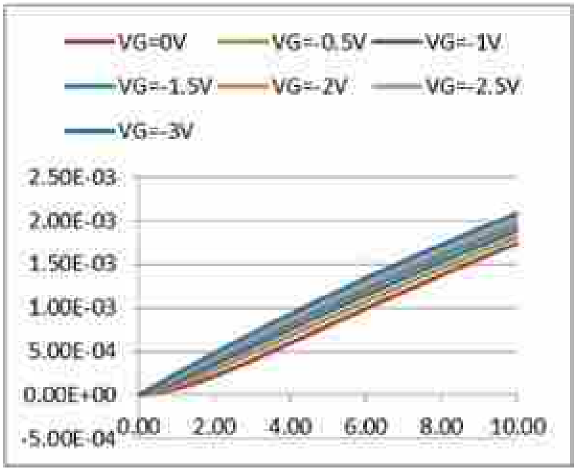


Fig.95: Ids vs Vds curves

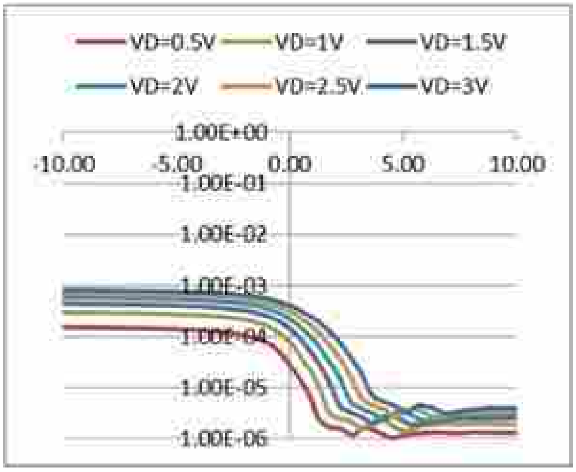


Fig.96: Ids vs Vgs curves

NW thickness 75nm:

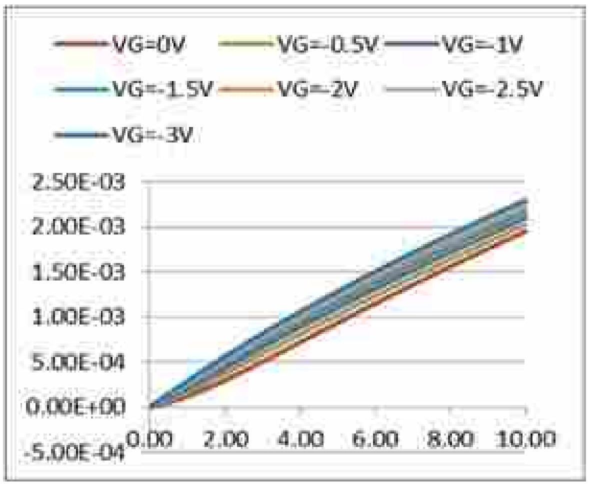


Fig.97: Ids vs Vds curves

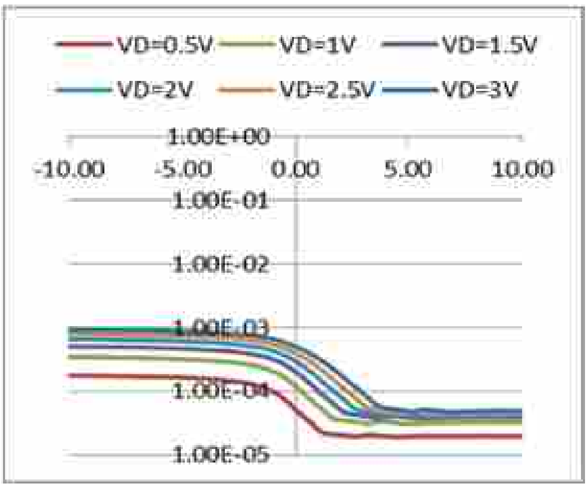


Fig.98: Ids vs Vgs curves

NW thickness 100nm:

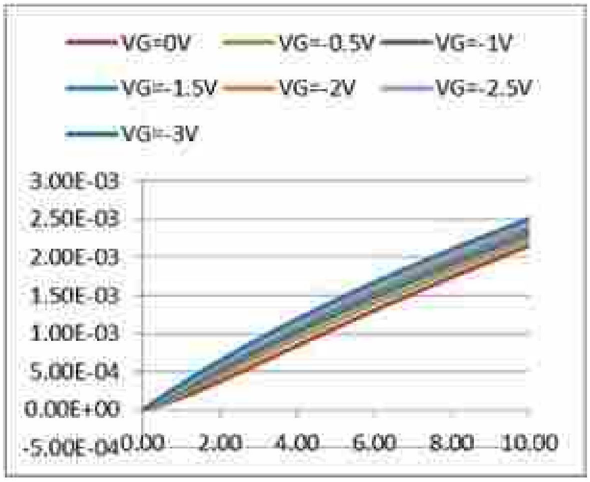


Fig.99: Ids vs Vds curves

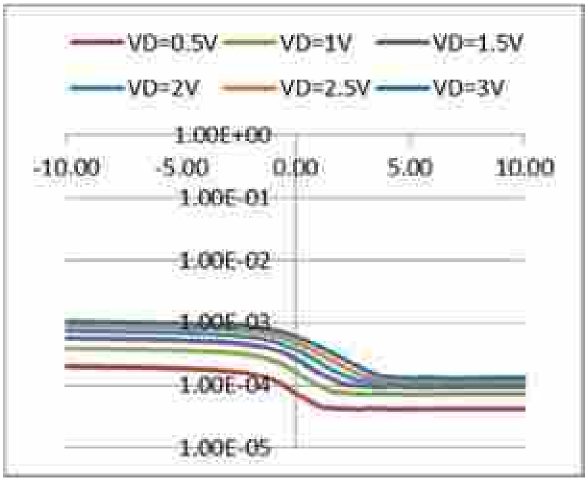


Fig.100: Ids vs Vgs curves

11. 1e18/cm^3

NW thickness 10nm:

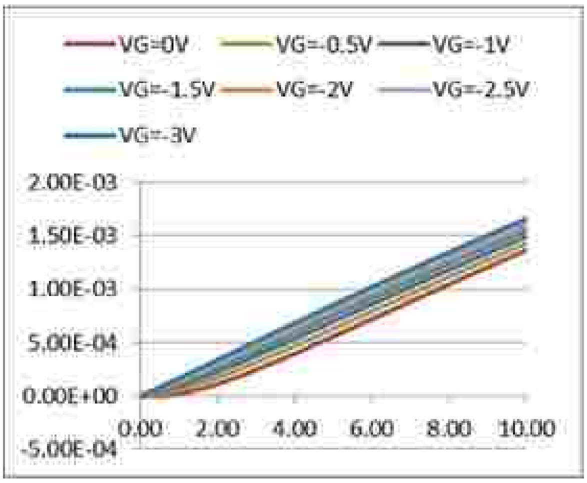


Fig.101: Ids vs Vds curves

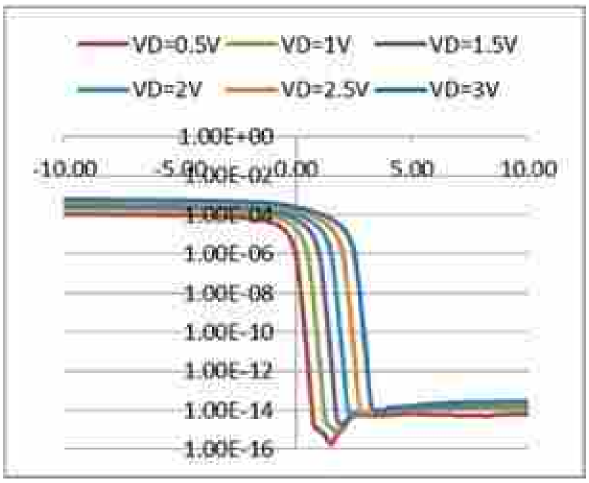


Fig.102: Ids vs Vgs curves

NW thickness 25nm:

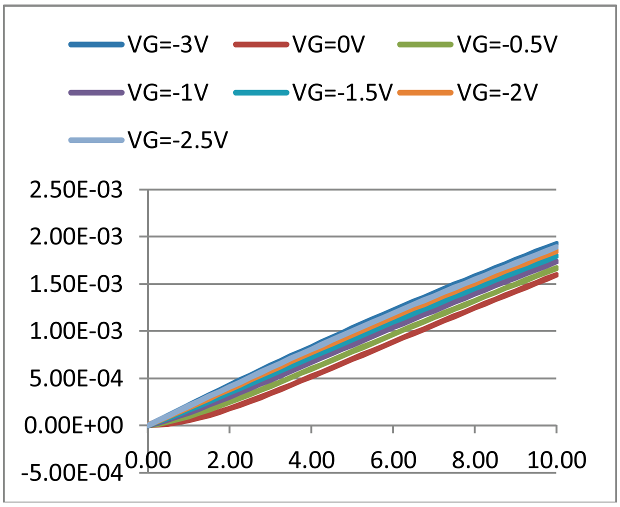


Fig.103: Ids vs Vds curves

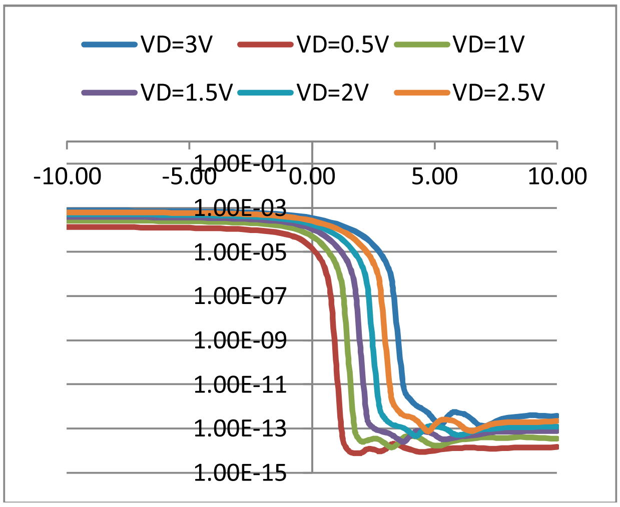


Fig.104: Ids vs Vgs curves

NW thickness 50nm:

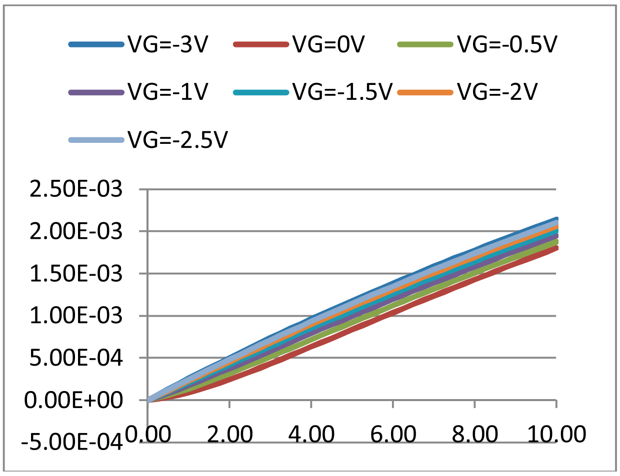


Fig.105: Ids vs Vds curves

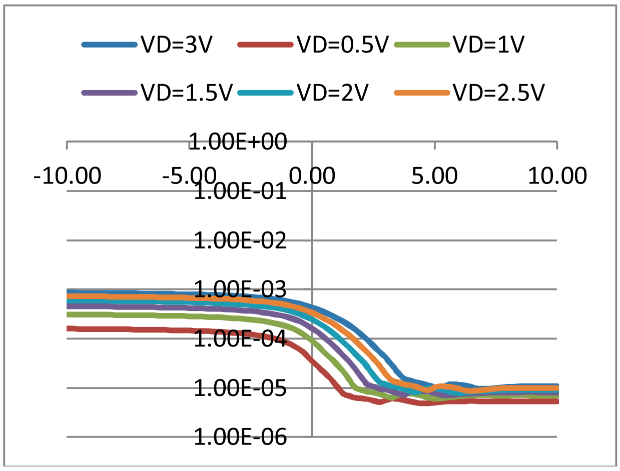


Fig.106: Ids vs Vgs curves

NW thickness 75nm:

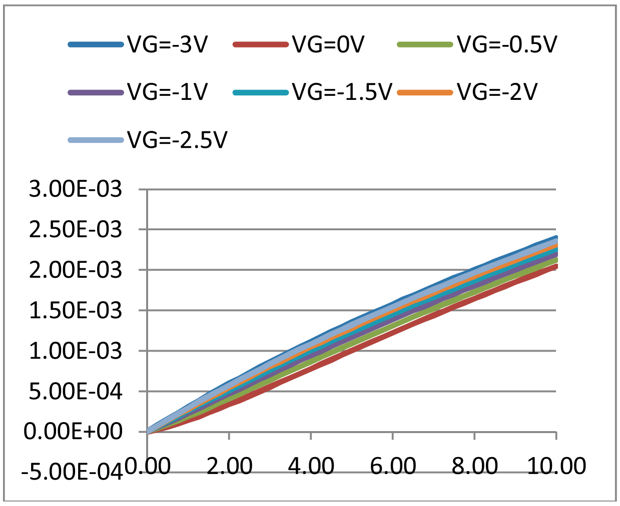


Fig.107: Ids vs Vds curves

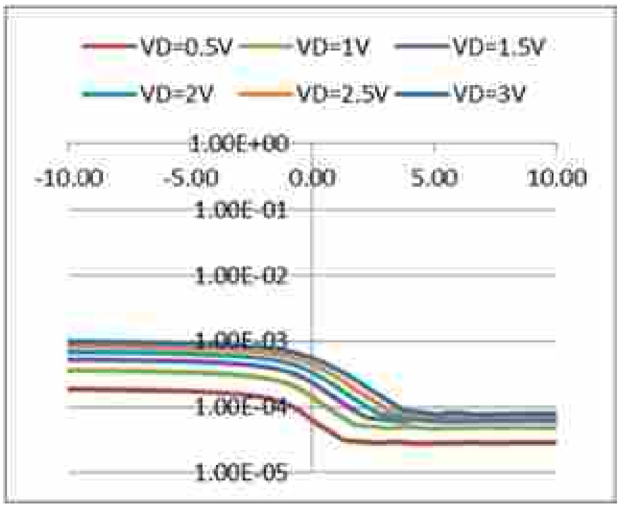


Fig.108: Ids vs Vgs curves

NW thickness 75nm:

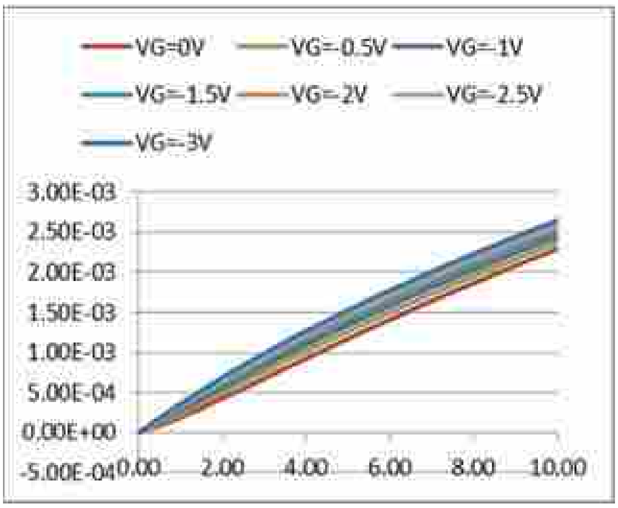


Fig.109: Ids vs Vds curves

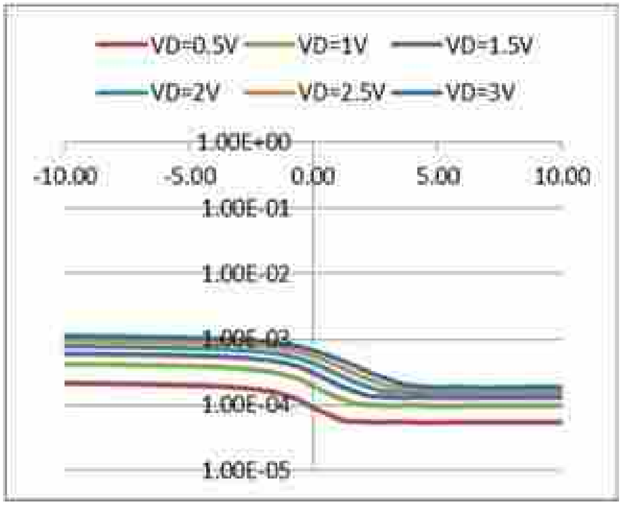


Fig.110: Ids vs Vgs curves

APPENDIX E: POLY SILICON NANOWIRE

1. 1e16/cm^3

NW thickness 10nm:

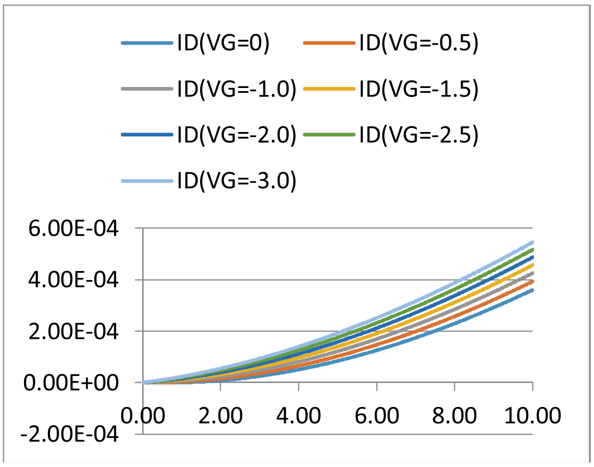


Fig.01: Ids vs Vds curves

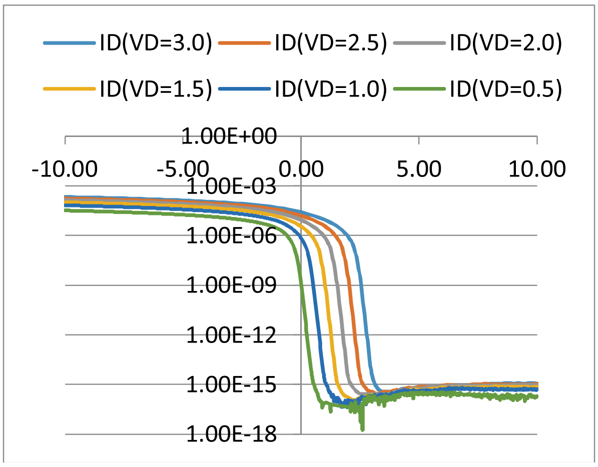


Fig.02: Ids vs Vgs curves

NW thickness 25nm:

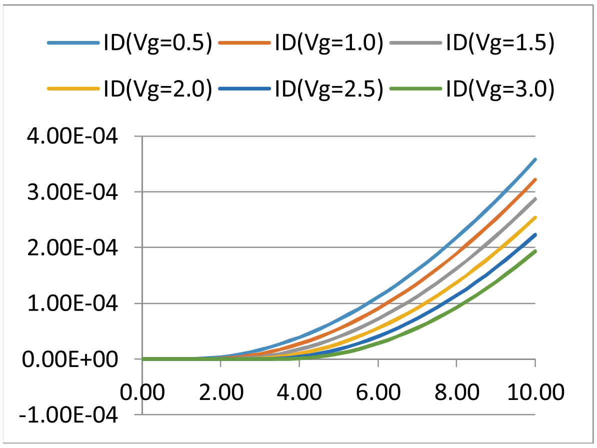


Fig.03: Ids vs Vds curves

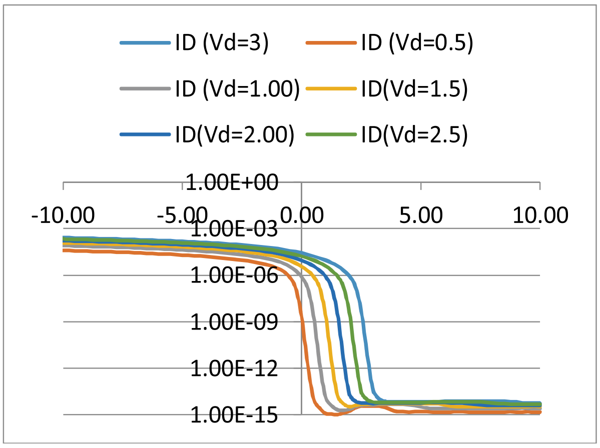


Fig.04: Ids vs Vgs curves

NW thickness 50nm:

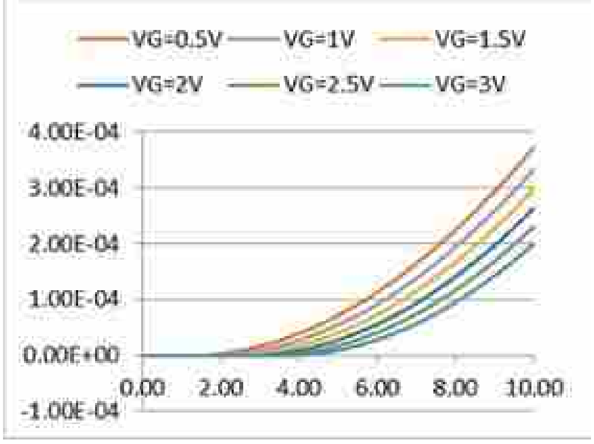


Fig.05: Ids vs Vds curves

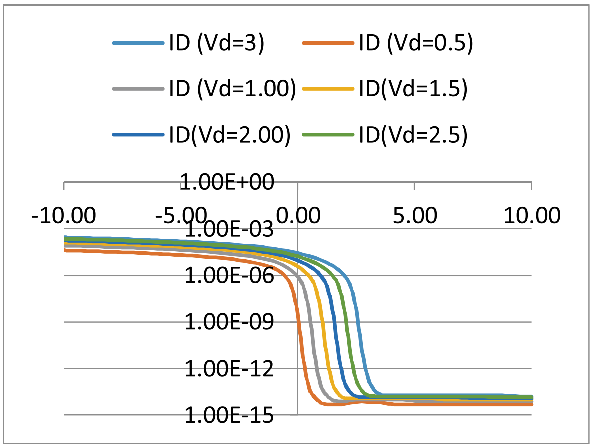


Fig.06: Ids vs Vgs curves

NW thickness 75nm:

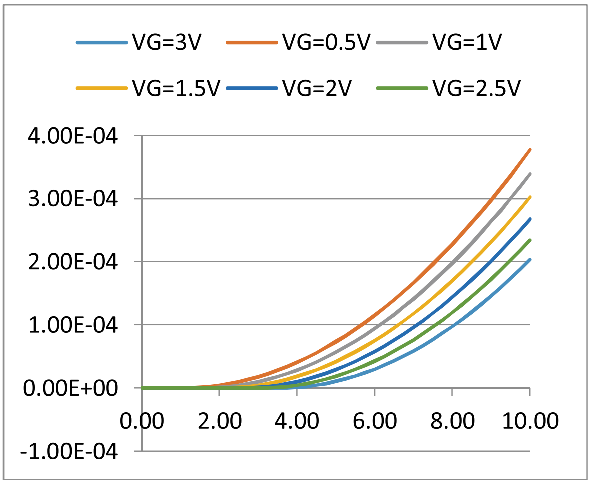


Fig.07: Ids vs Vds curves

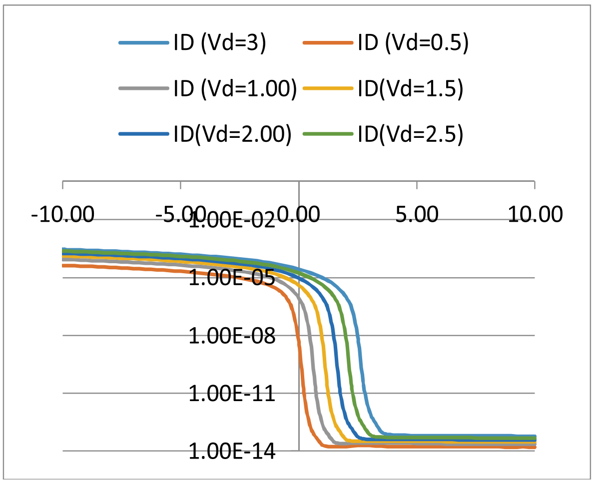


Fig.08: Ids vs Vgs curves

NW thickness 100nm:

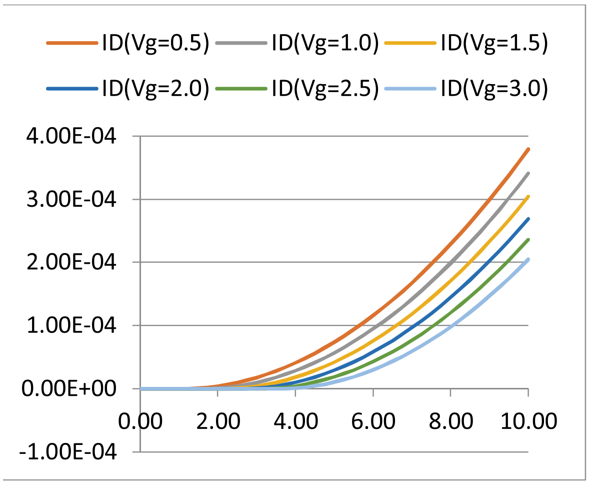


Fig.09: Ids vs Vds curves

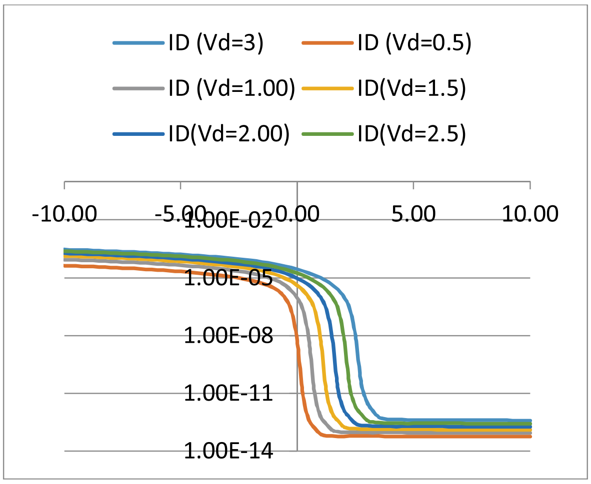


Fig.10: Ids vs Vgs curves

2. 2e16/cm^3

NW thickness 10nm:

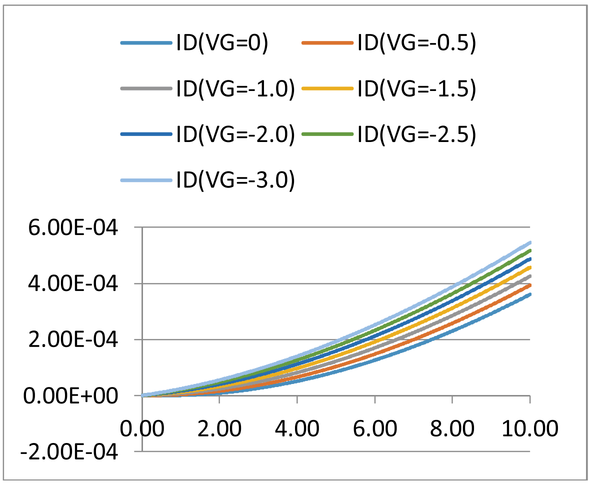


Fig.11: Ids vs Vds curves

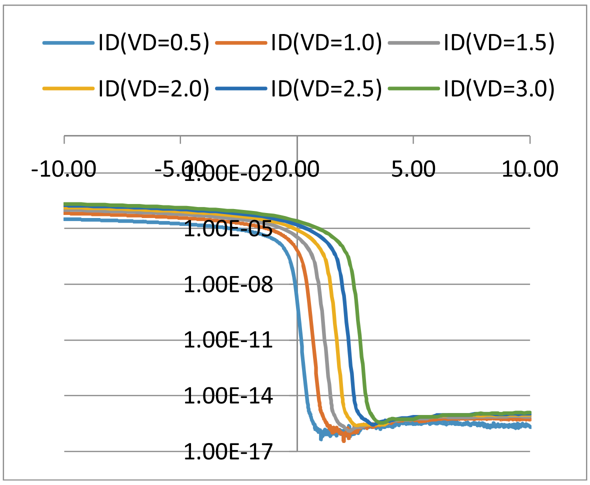


Fig.12: Ids vs Vgs curves

NW thickness 25nm:

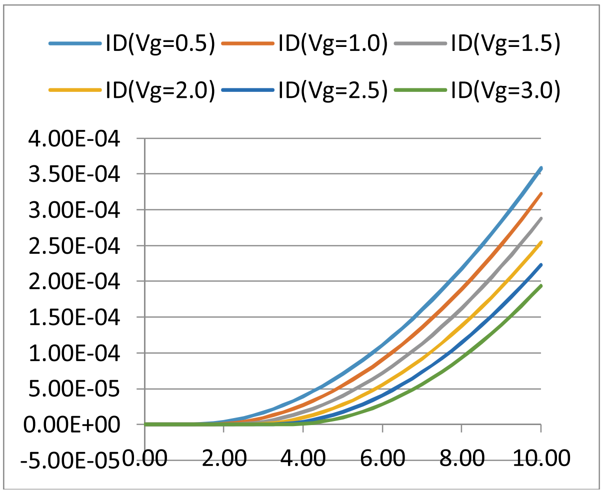


Fig.13: Ids vs Vds curves

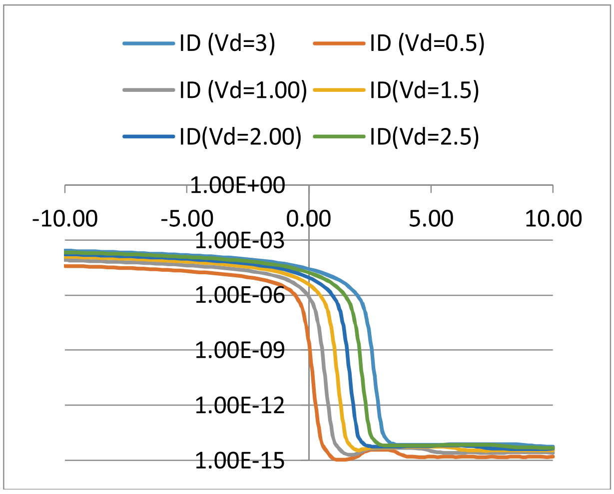


Fig.14: Ids vs Vgs curves

NW thickness 50nm:

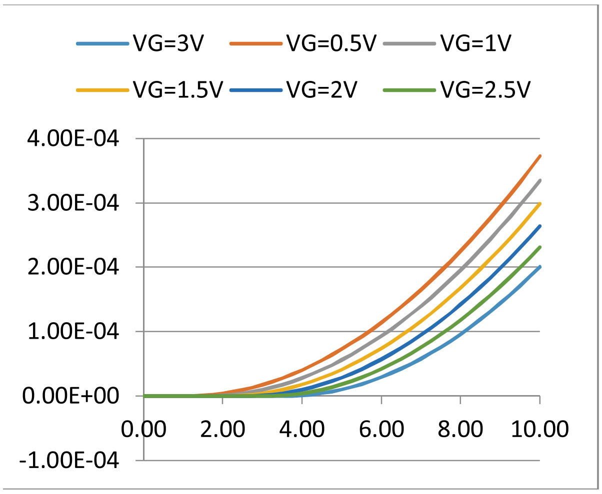


Fig.15: Ids vs Vds curves

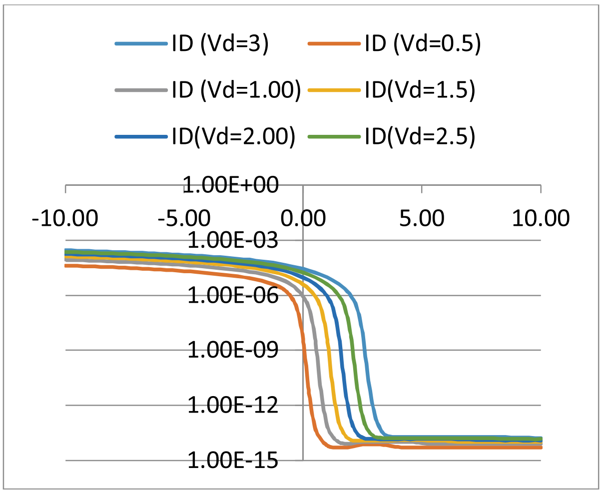


Fig.16: Ids vs Vgs curves

NW thickness 75nm:

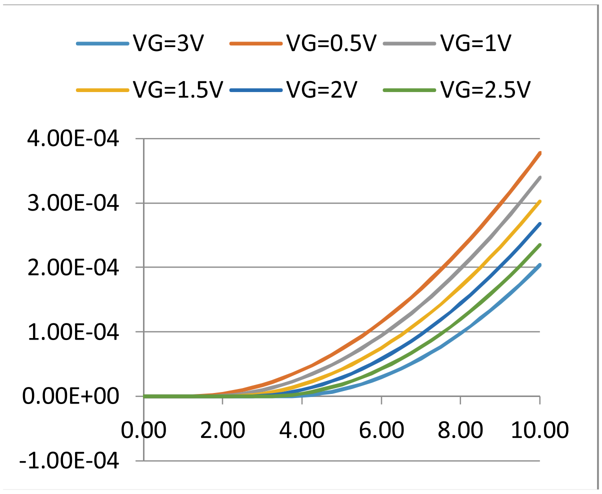


Fig.17: Ids vs Vds curves

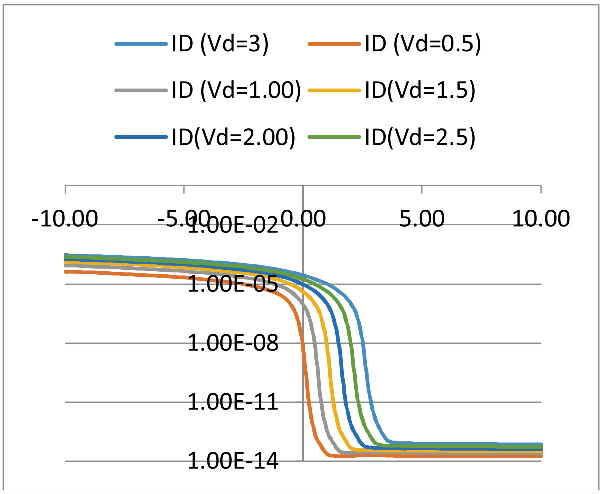


Fig.18: Ids vs Vgs curves

NW thickness 100nm:

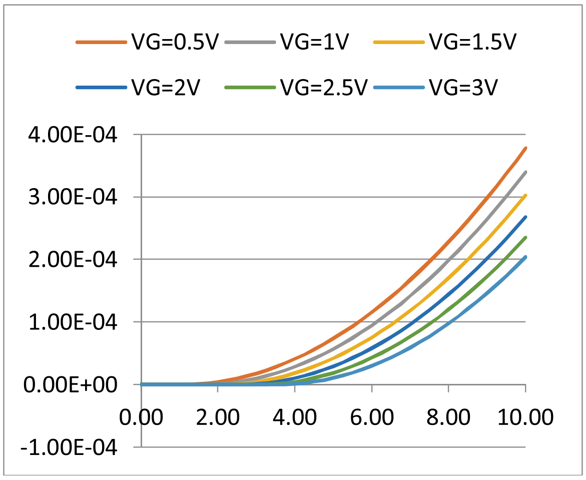


Fig.19: Ids vs Vds curves

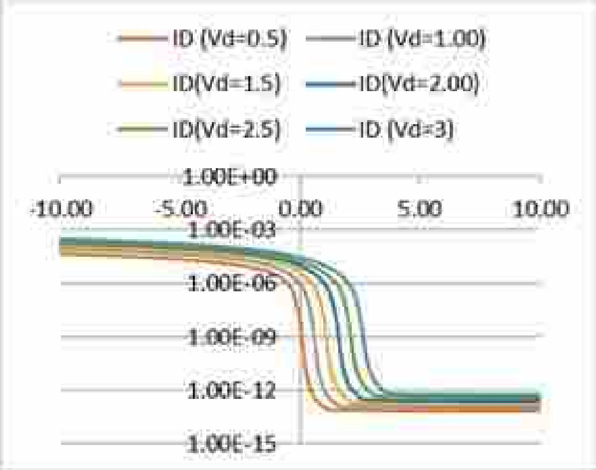


Fig.20: Ids vs Vgs curves

3. 4e16/cm^3

NW thickness 10nm:

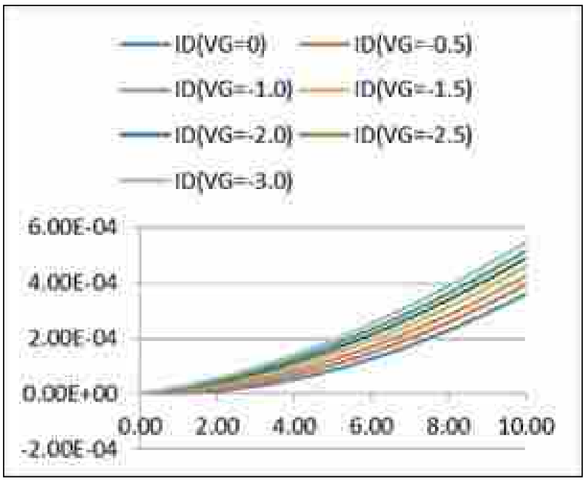


Fig.21: Ids vs Vds curves

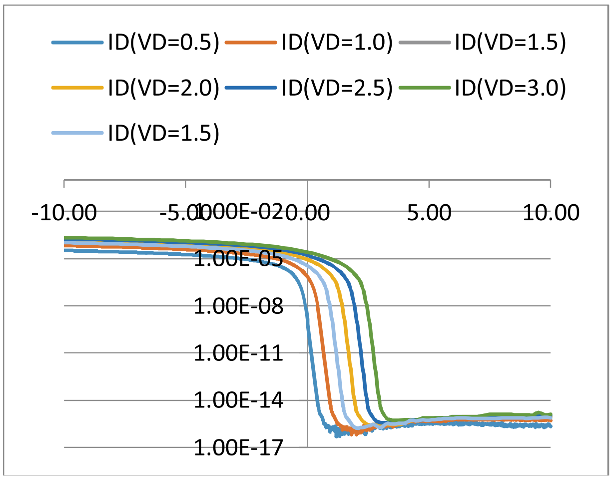


Fig.22: Ids vs Vgs curves

NW thickness 25nm:

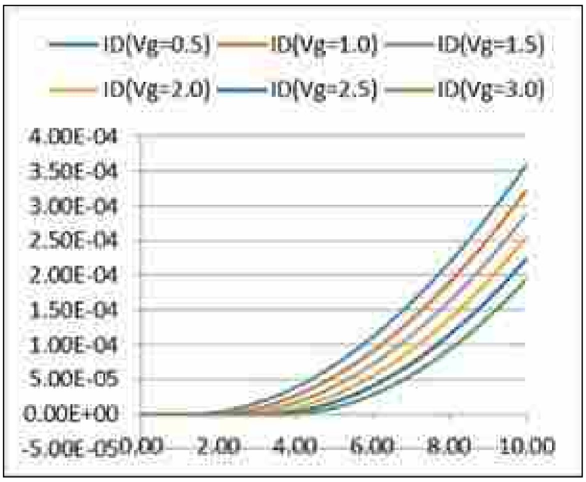


Fig.23: Ids vs Vds curves

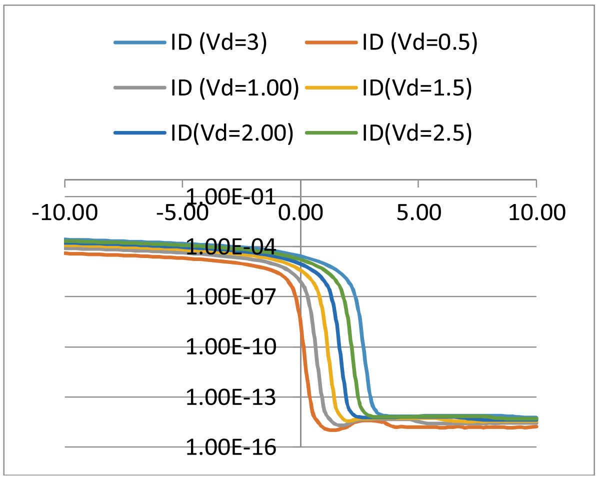


Fig.24: Ids vs Vgs curves

NW thickness 50nm:

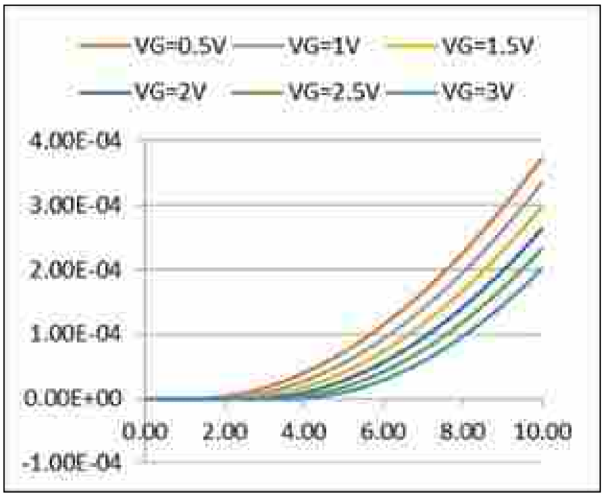


Fig.25: Ids vs Vds curves

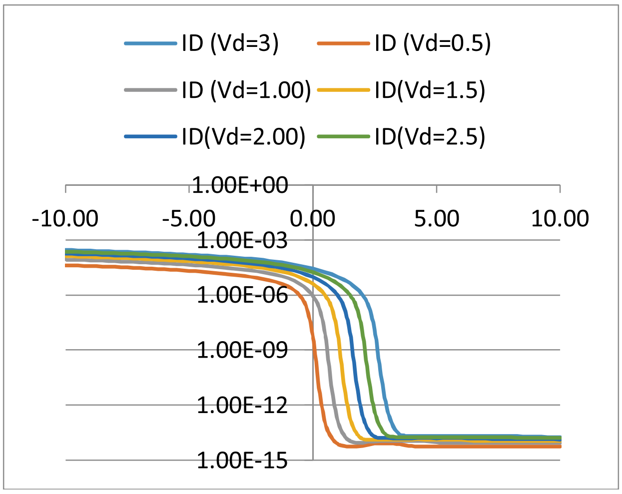


Fig.26: Ids vs Vgs curves

NW thickness 75nm:

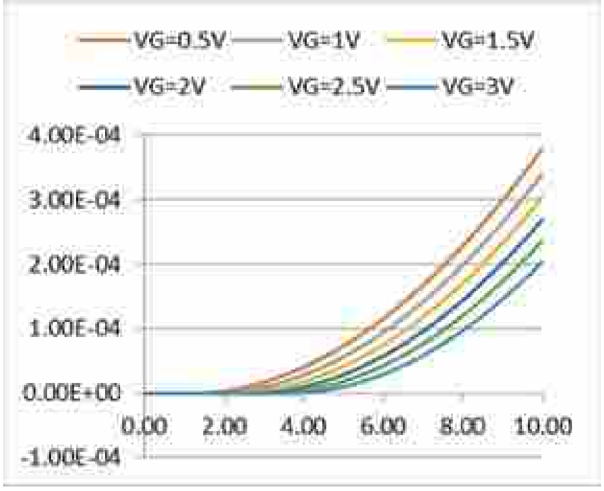


Fig.27: Ids vs Vds curves

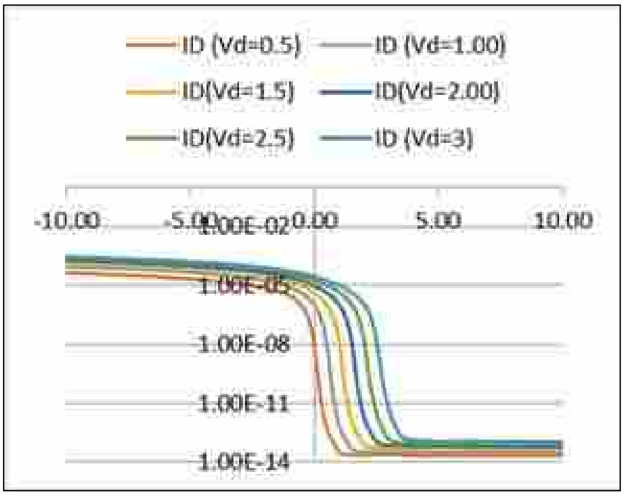


Fig.28: Ids vs Vgs curves

NW thickness 100nm:

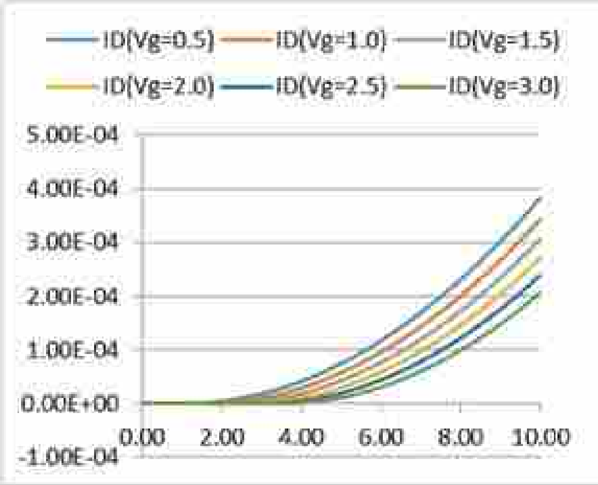


Fig.29: Ids vs Vds curves

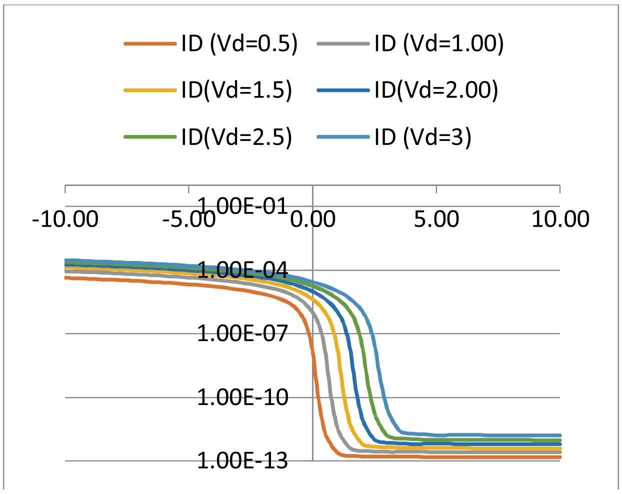


Fig.30: Ids vs Vgs curves

4. 6e16/cm^3

NW thickness 10nm:

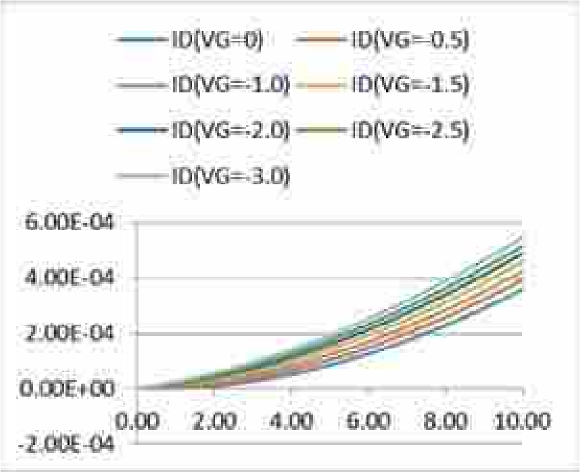


Fig.31: Ids vs Vds curves

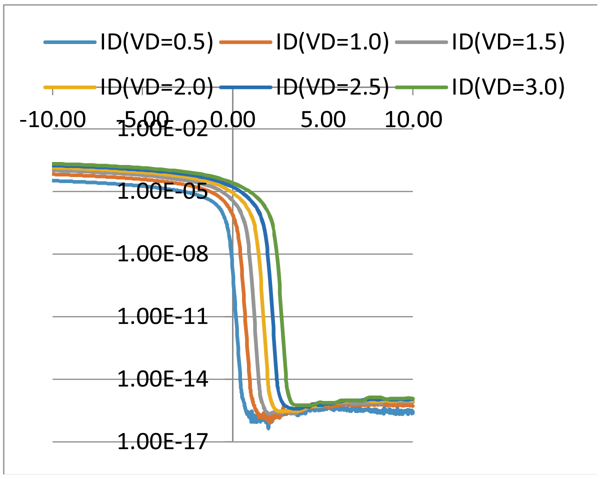
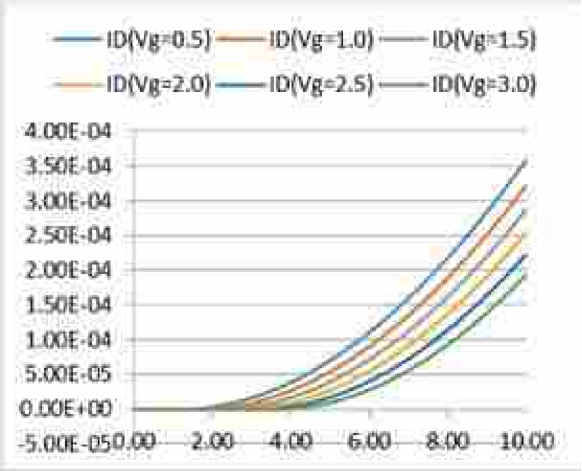


Fig.32: Ids vs Vgs curves

NW thickness 25nm:



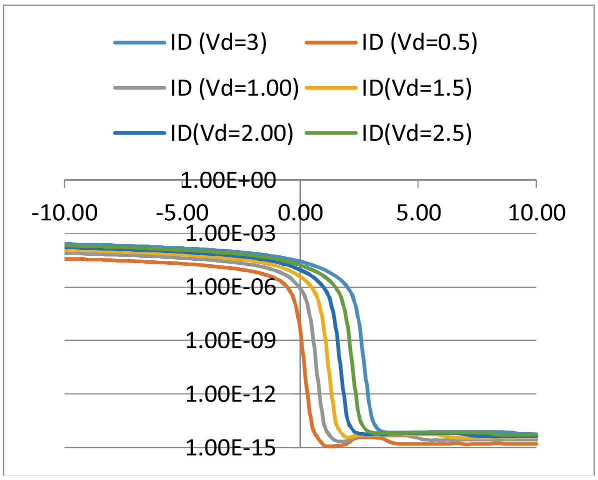
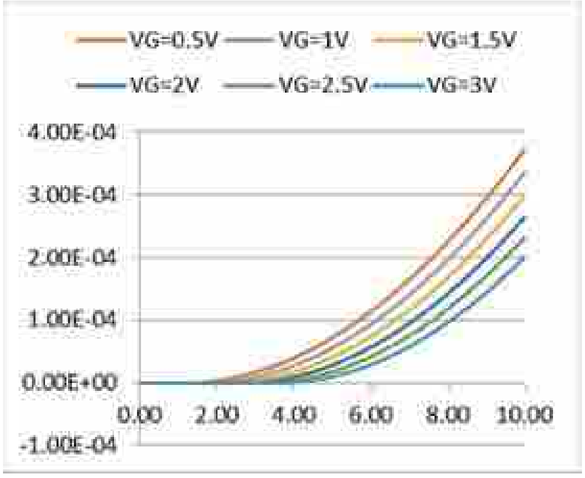


Fig.33: Ids vs Vds curves

Fig.34: Ids vs Vgs curves

NW thickness 50nm:



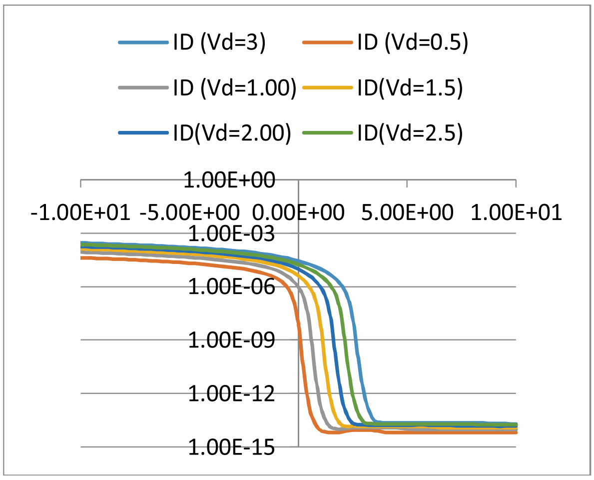


Fig.35: Ids vs Vds curves

Fig.36: Ids vs Vgs curves

NW thickness 75nm:

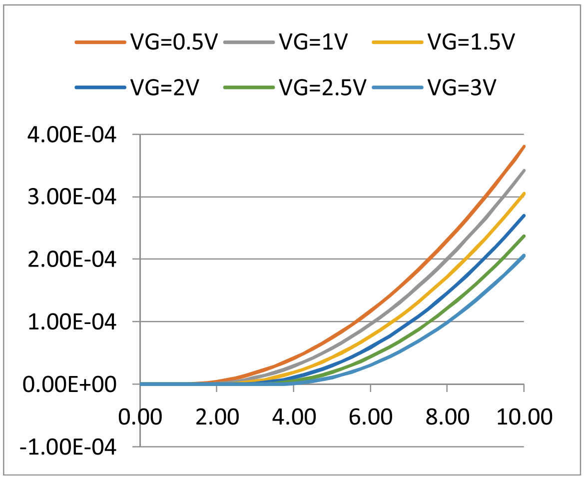


Fig.37: Ids vs Vds curves

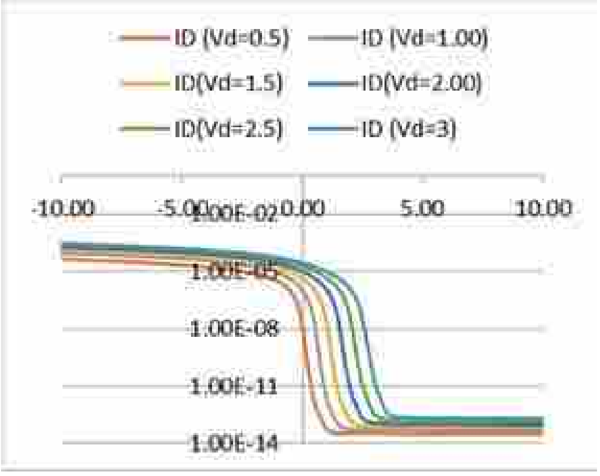


Fig.38: Ids vs Vgs curves

NW thickness 100nm:

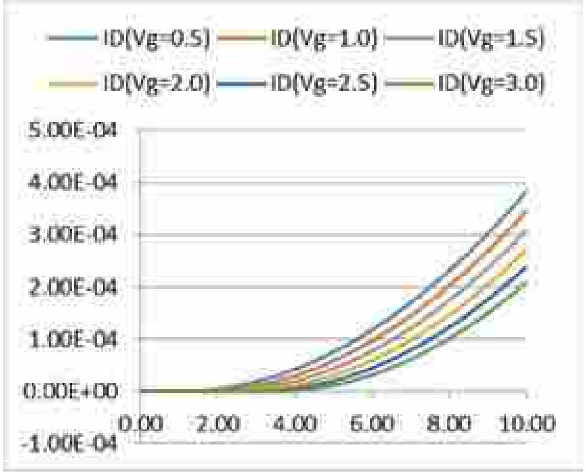


Fig.39: Ids vs Vds curves

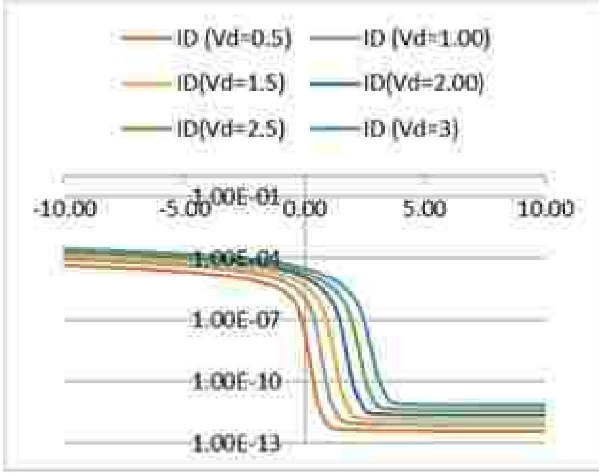


Fig.40: Ids vs Vgs curves

5. 8e16/cm^3

NW thickness 10nm:

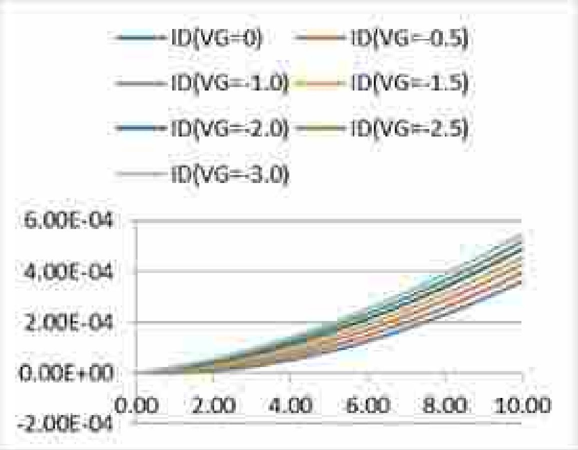


Fig.41: Ids vs Vds curves

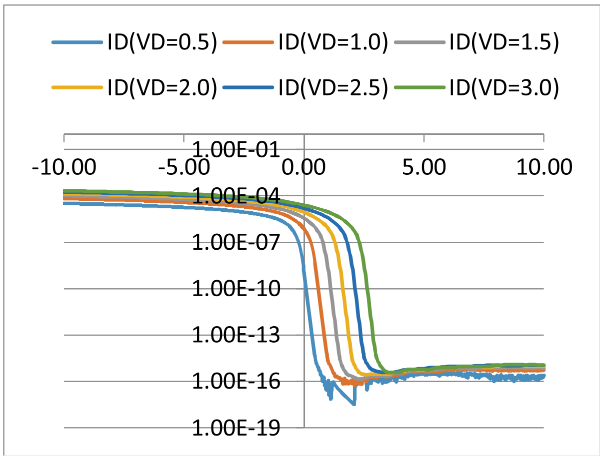


Fig.42: Ids vs Vgs curves

NW thickness 25nm:

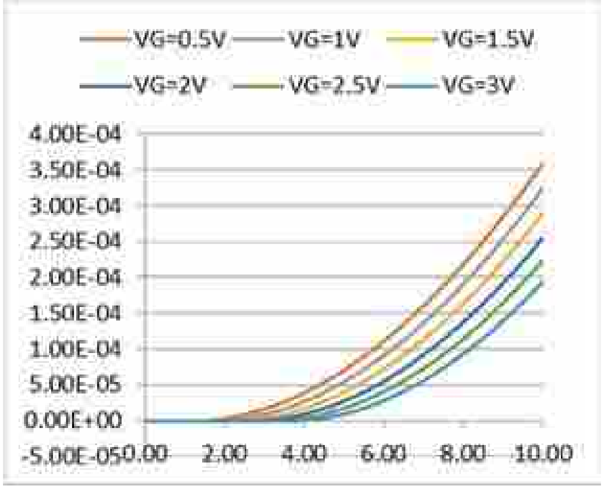


Fig.43: Ids vs Vds curves

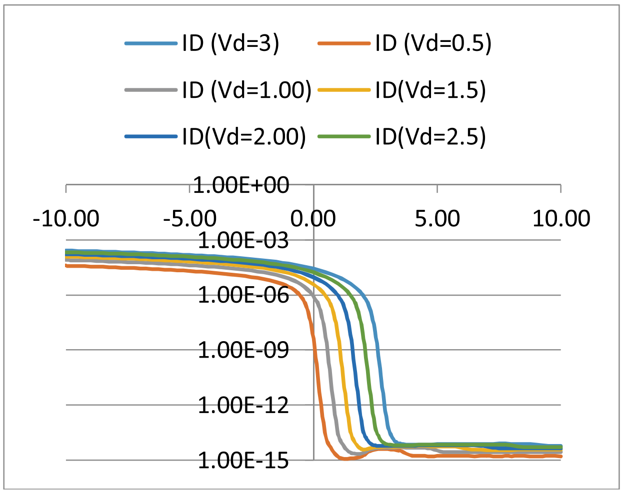


Fig.44: Ids vs Vgs curves

NW thickness 50nm:

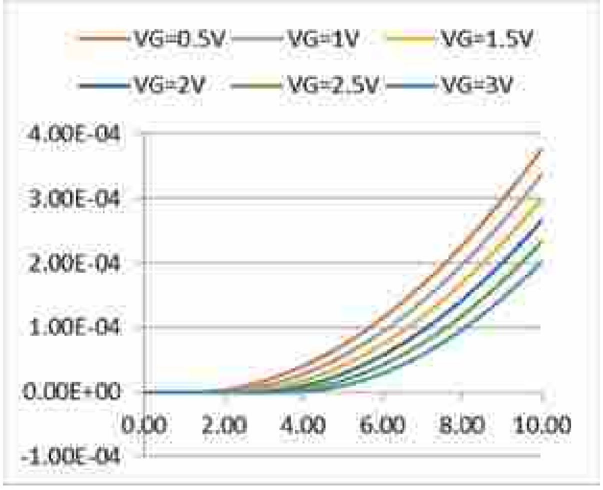


Fig.45: Ids vs Vds curves

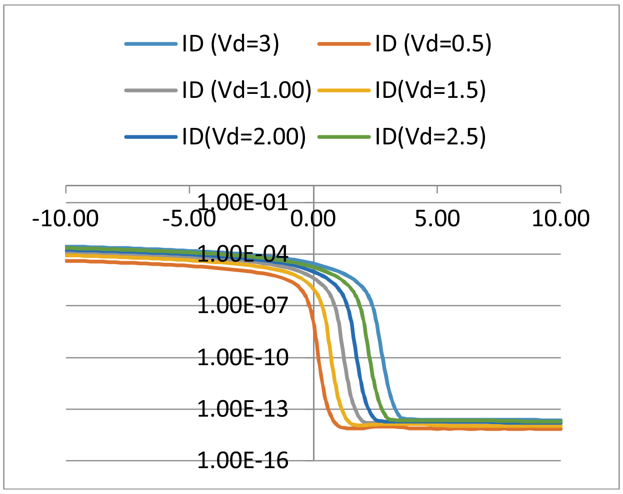


Fig.46: Ids vs Vgs curves

NW thickness 75nm:

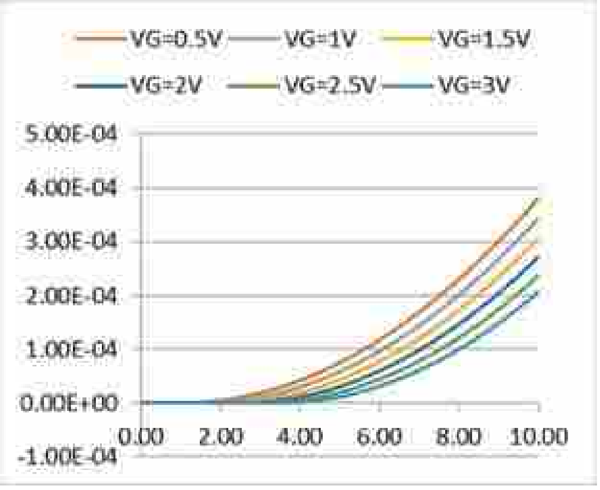


Fig.47: Ids vs Vds curves

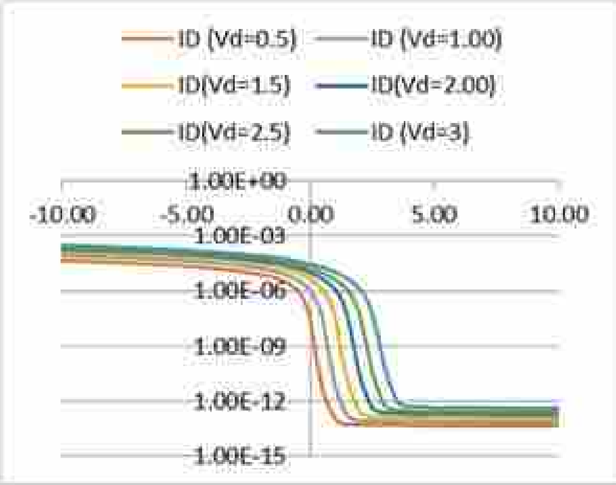


Fig.48: Ids vs Vgs curve

NW thickness 100nm:

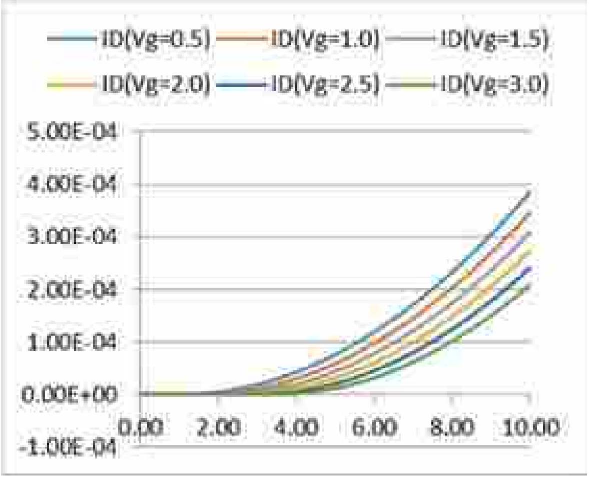


Fig.49: Ids vs Vds curves

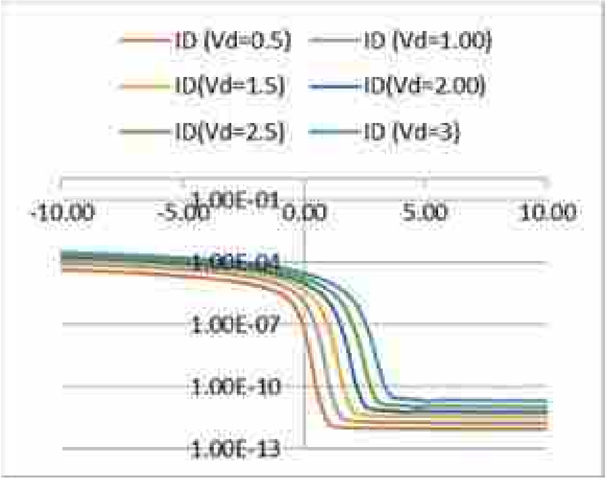


Fig.50: Ids vs Vgs curves

6. 1e17/cm^3

NW thickness 10nm:

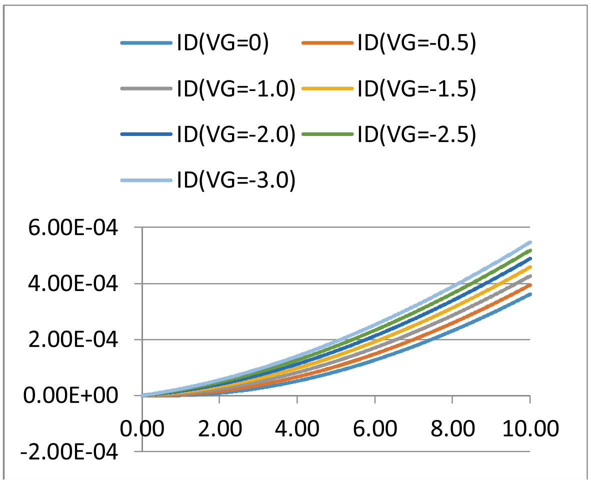


Fig.51: Ids vs Vds curves

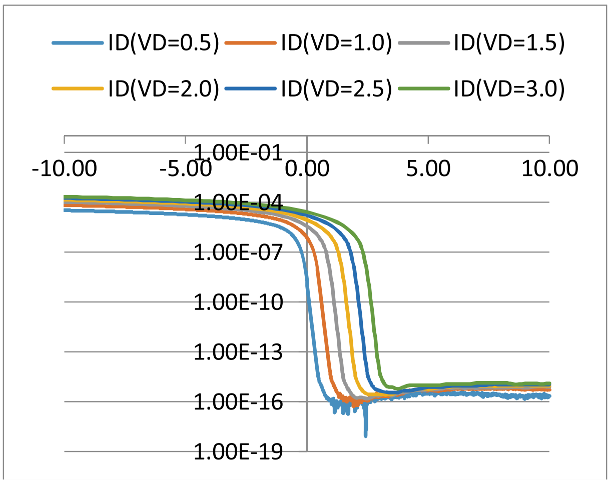


Fig.52: Ids vs Vgs curves

NW thickness 25nm:

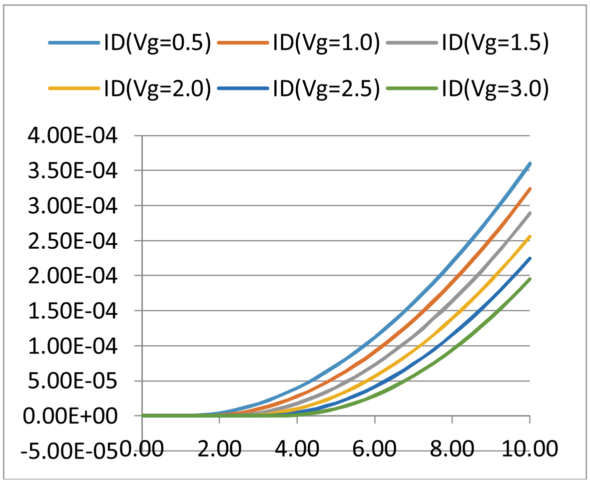


Fig.53: Ids vs Vds curves

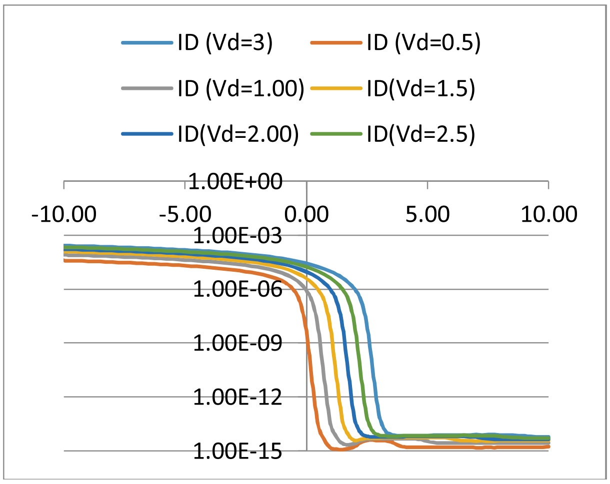


Fig.54: Ids vs Vgs curves

NW thickness 50nm:

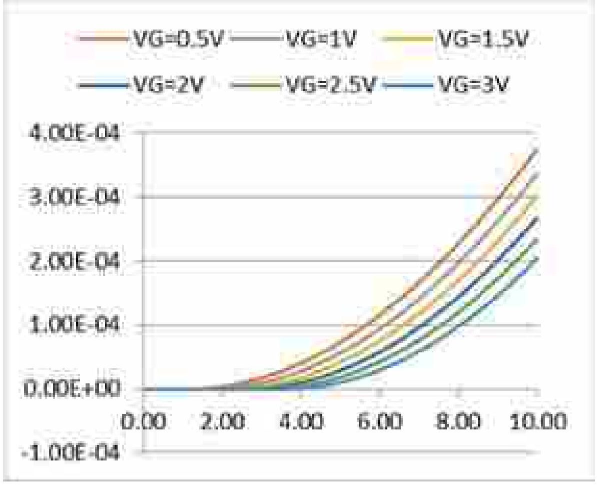


Fig.55: Ids vs Vds curves

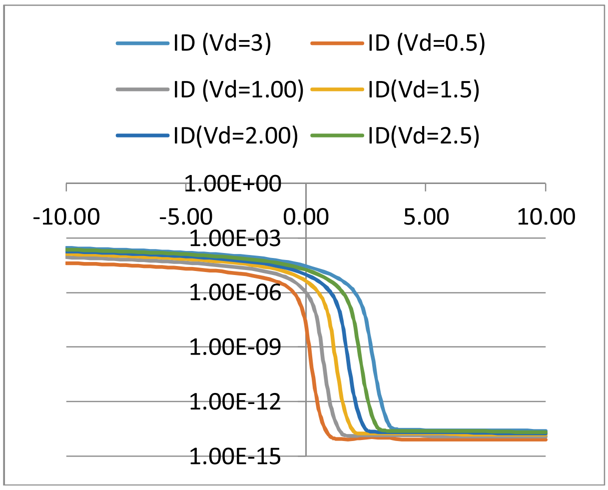


Fig.56: Ids vs Vgs curves

NW thickness 75nm:

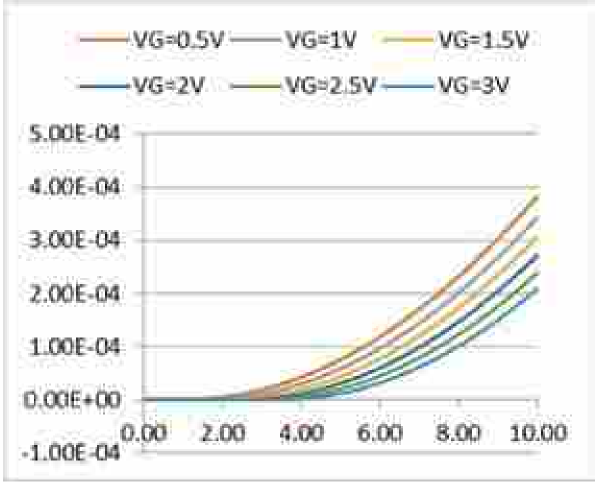


Fig.57: Ids vs Vds curves

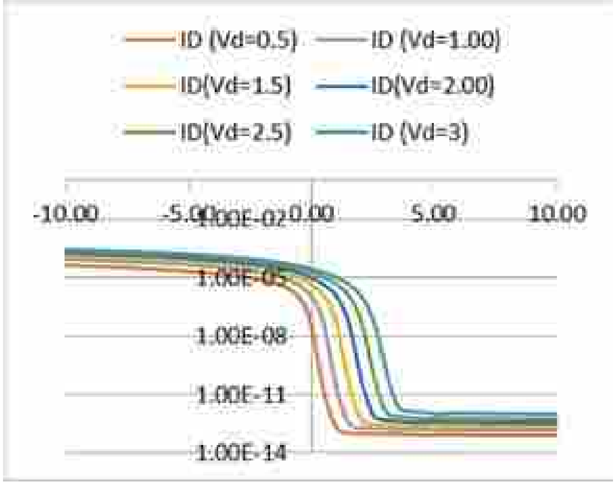


Fig.58: Ids vs Vgs curves

NW thickness 100nm:

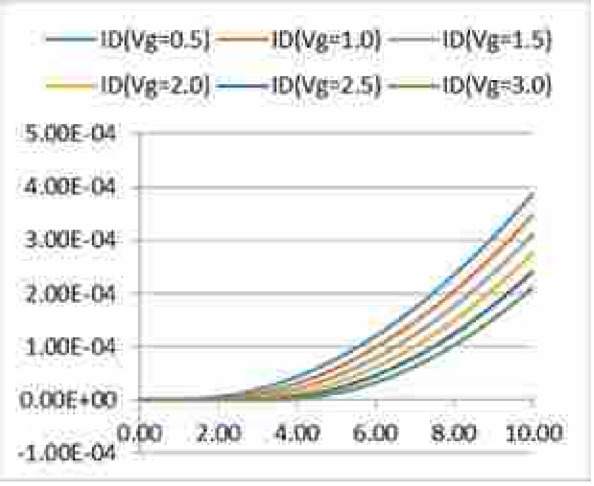


Fig.59: Ids vs Vds curves

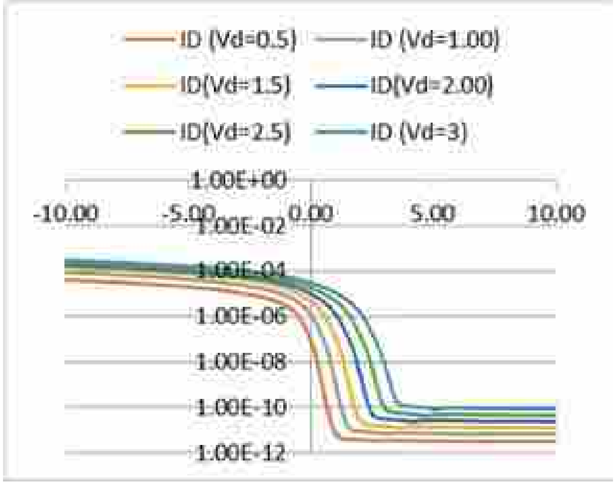


Fig.60: Ids vs Vgs curves

7. 2e17/cm^3

NW thickness 10nm:

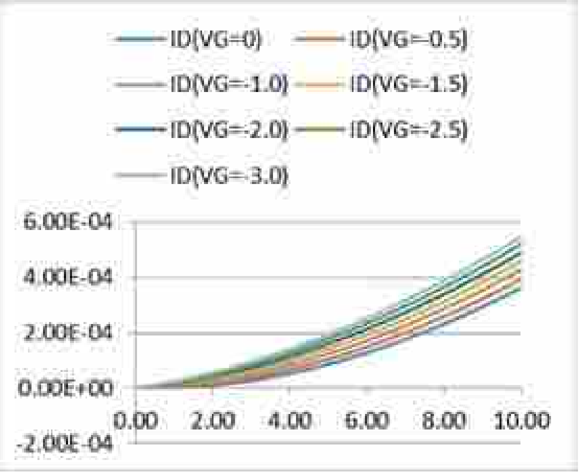


Fig.61: Ids vs Vds curves

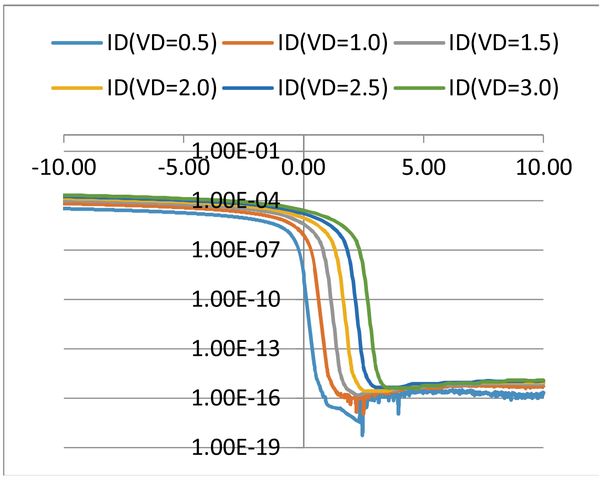


Fig.62: Ids vs Vgs curves

NW thickness 25nm:

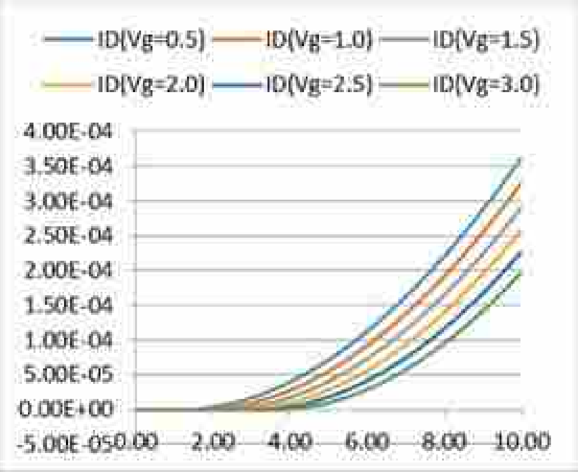


Fig.63: Ids vs Vds curves

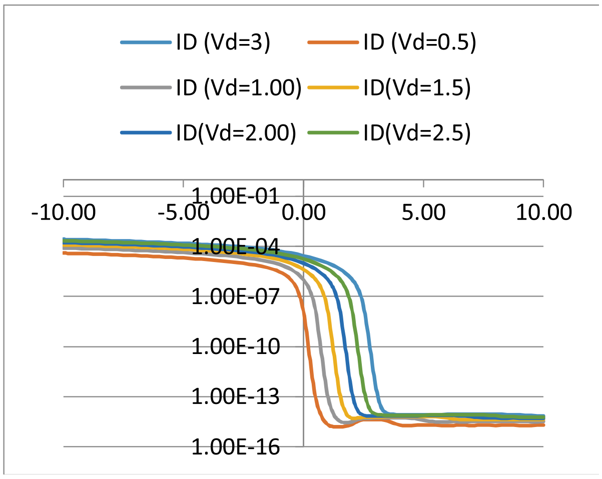


Fig.64: Ids vs Vgs curves

NW thickness 50nm:

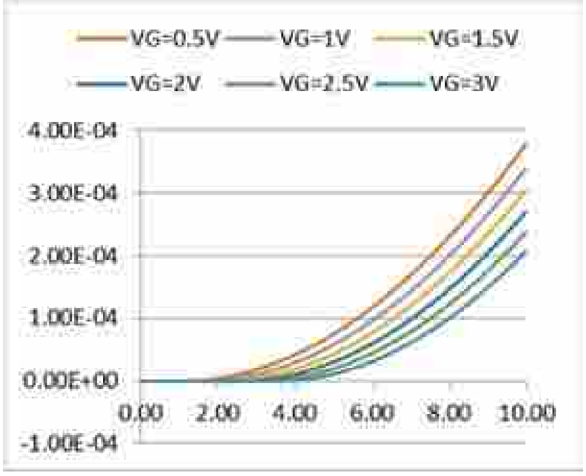


Fig.65: Ids vs Vds curves

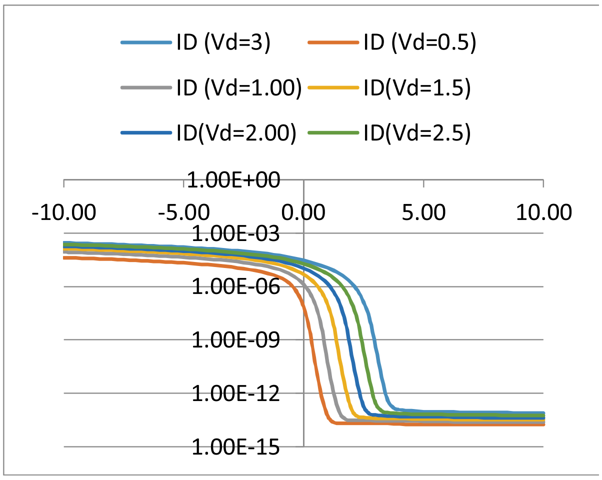


Fig.66: Ids vs Vgs curves

NW thickness 75nm:

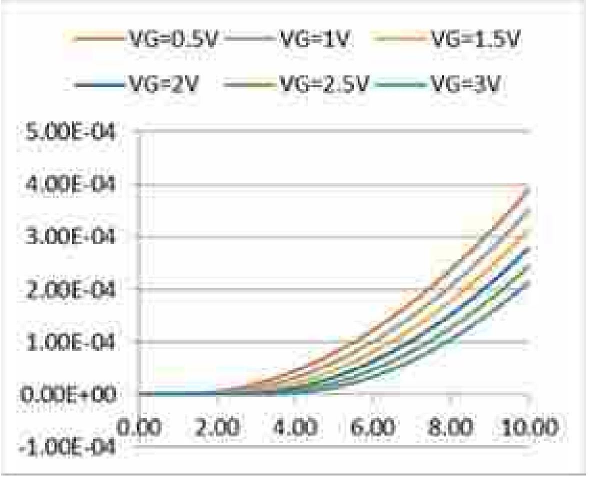


Fig.67: Ids vs Vds curves

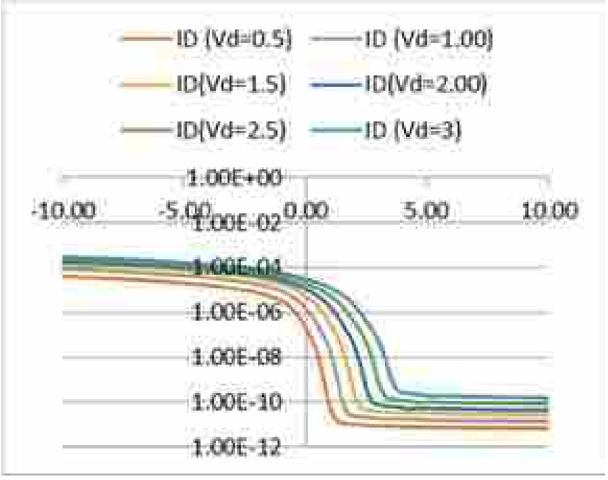


Fig.68: Ids vs Vgs curve

NW thickness 100nm:

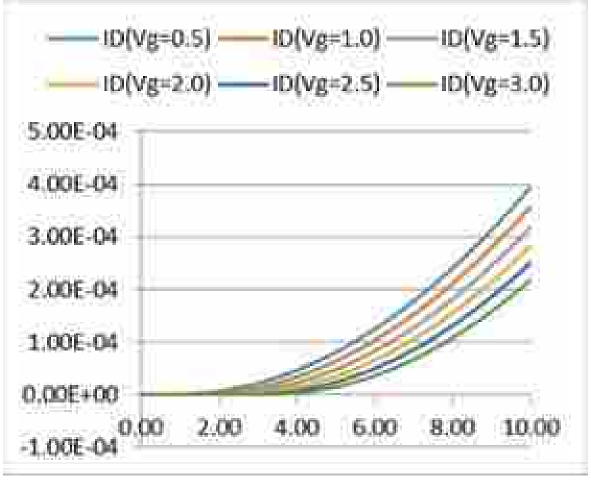


Fig.69: Ids vs Vds curves

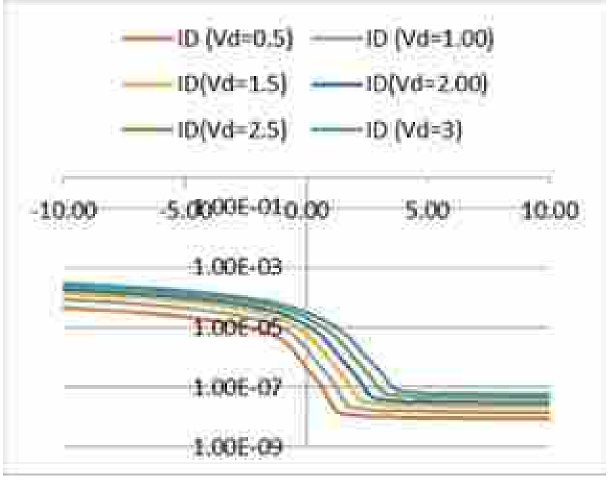


Fig.70: Ids vs Vgs curves

8. 4e17/cm^3

NW thickness 10nm:

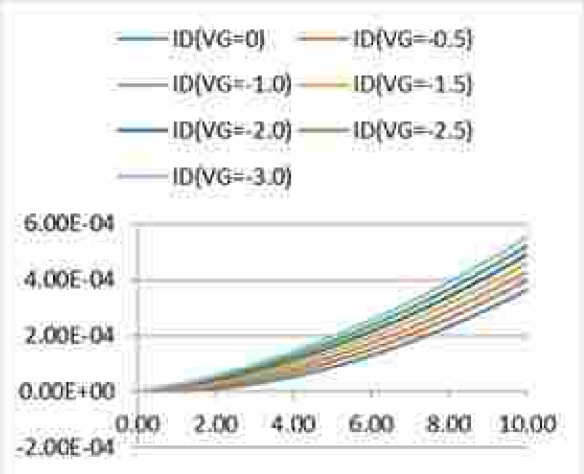


Fig.71: Ids vs Vds curves

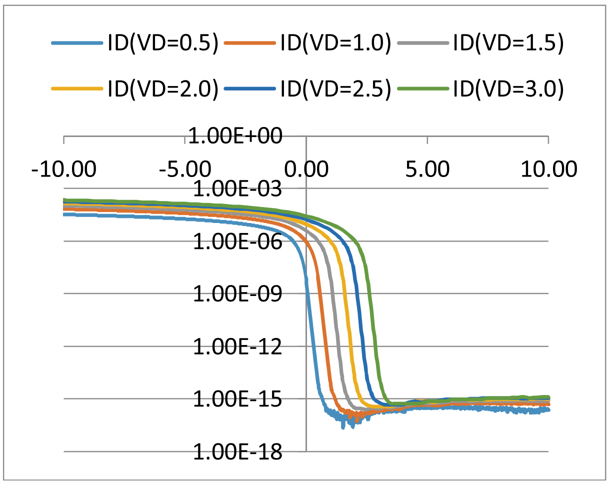


Fig.72: Ids vs Vgs curves

NW thickness 25nm:

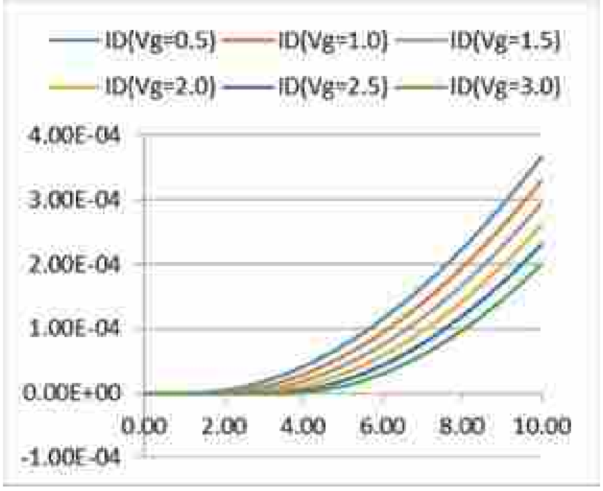


Fig.73: Ids vs Vds curves

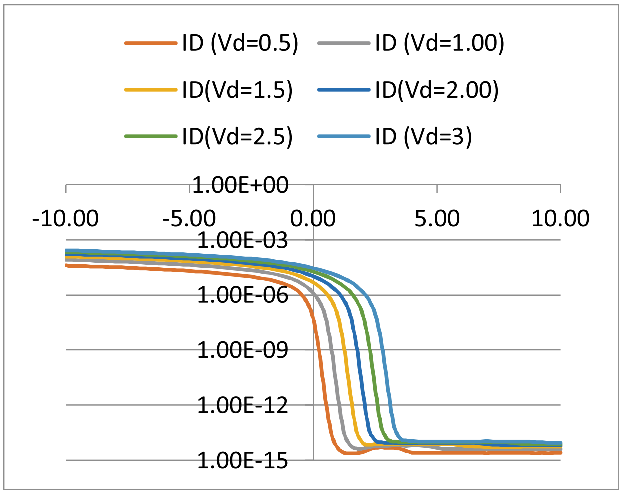


Fig.74: Ids vs Vgs curves

NW thickness 50nm:

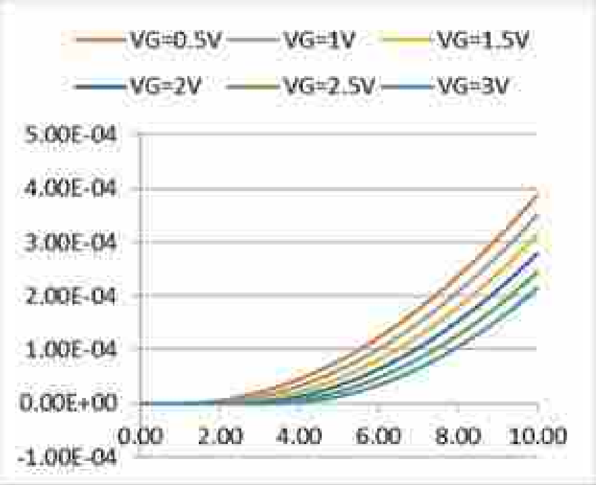


Fig.75: Ids vs Vds curves

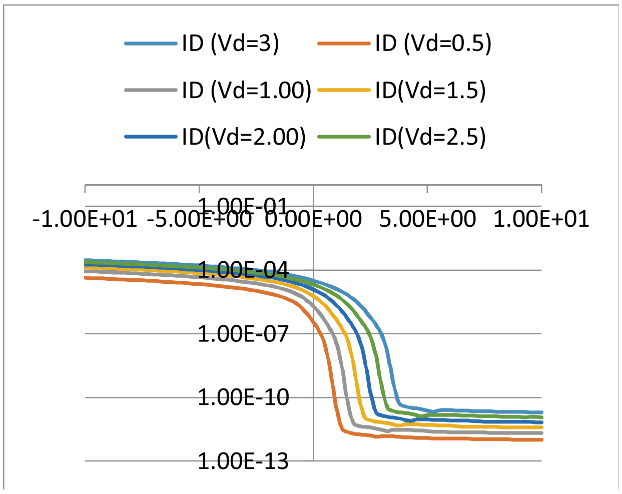


Fig.76: Ids vs Vgs curves

NW thickness 75nm:

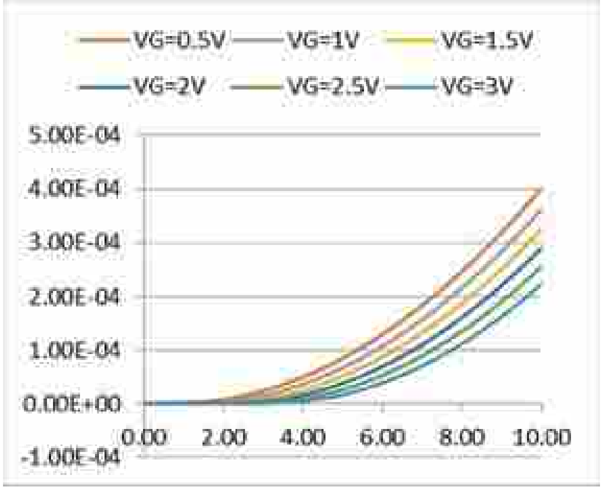


Fig.77: Ids vs Vds curves

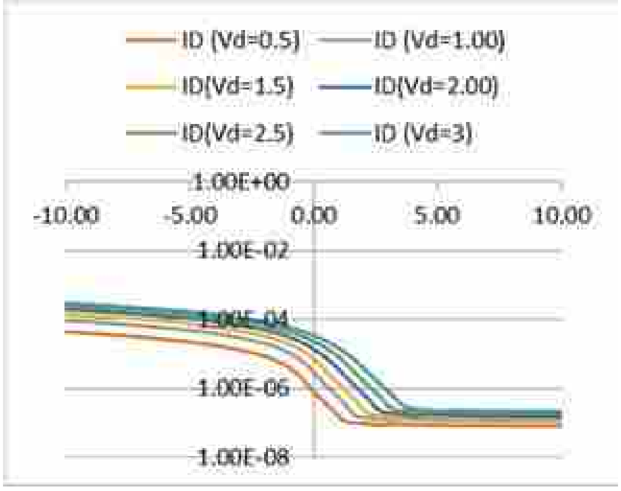


Fig.78: Ids vs Vgs curves

NW thickness 100nm:

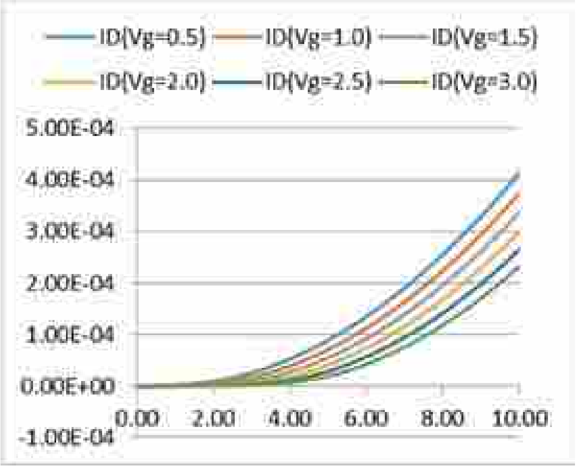


Fig.79: Ids vs Vds curves

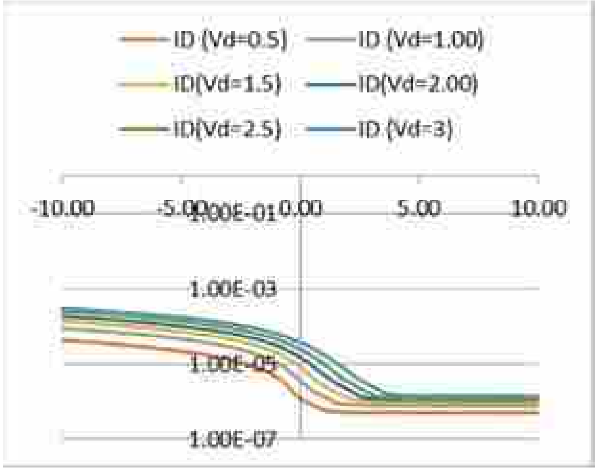


Fig.80: Ids vs Vgs curves

9. 6e17/cm^3

NW thickness 10nm:

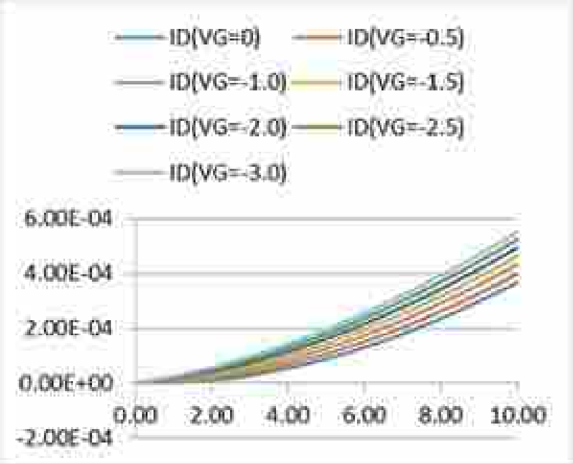


Fig.81: Ids vs Vds curves

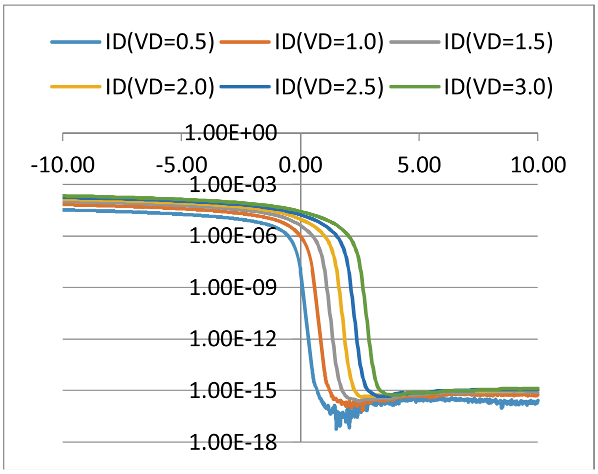


Fig.82: Ids vs Vgs curves

NW thickness 25m:

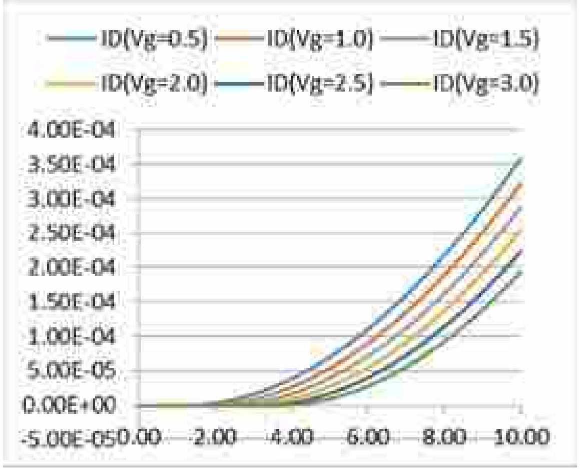


Fig.83: Ids vs Vds curves

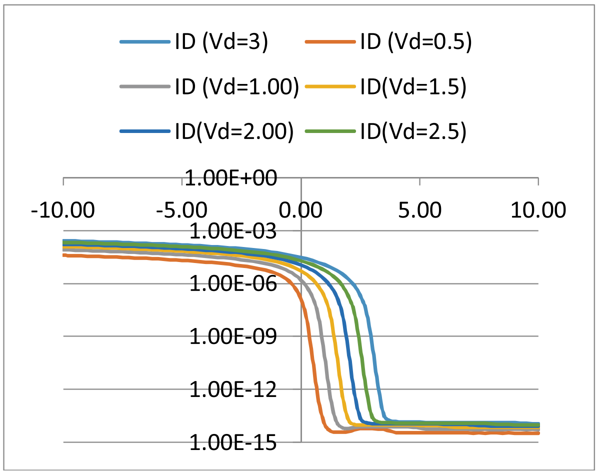


Fig.84: Ids vs Vgs curves

NW thickness 50m:

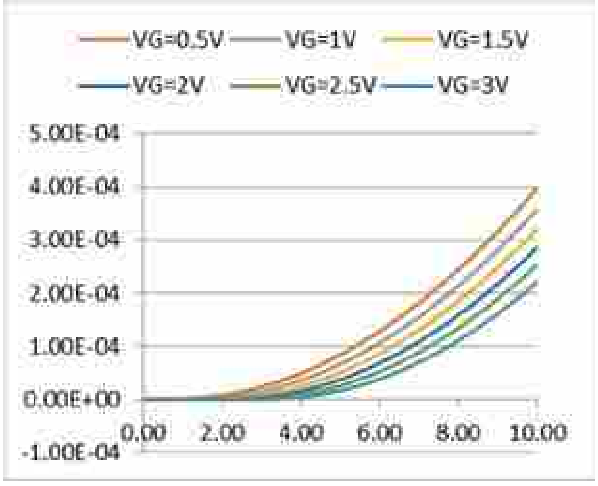


Fig.85: Ids vs Vds curves

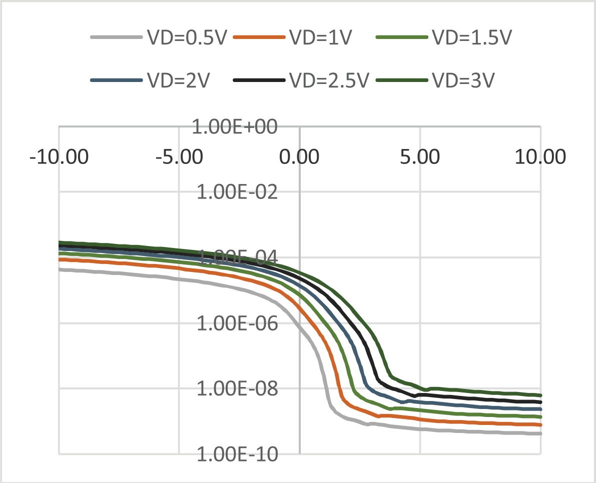


Fig.86: Ids vs Vgs curves

NW thickness 75m:

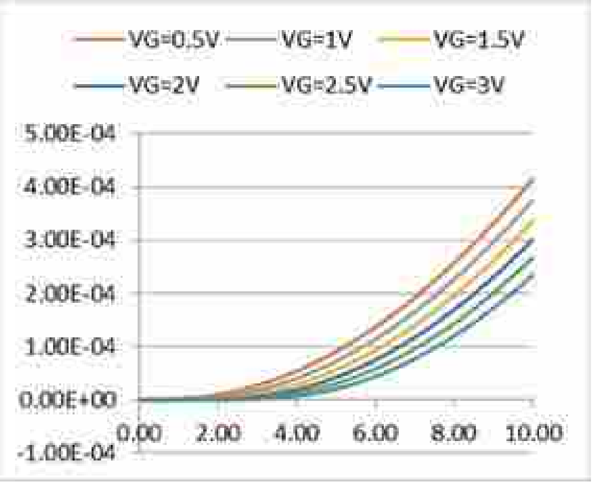


Fig.87: Ids vs Vds curves

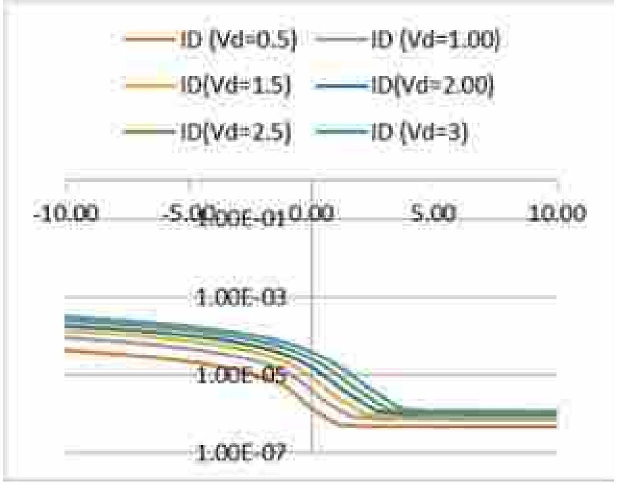


Fig.88: Ids vs Vgs curves

NW thickness 100m:

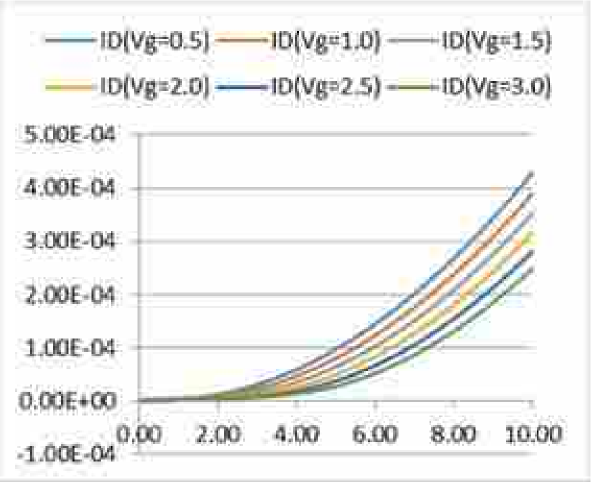


Fig.89: Ids vs Vds curves

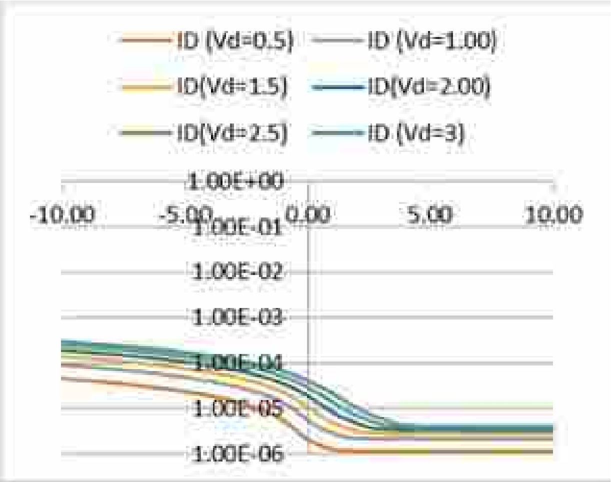


Fig.90: Ids vs Vgs curves

10. 8e17/cm^3

NW thickness 10nm:

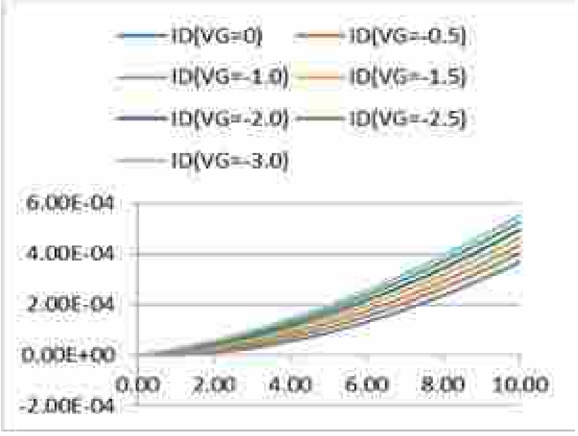


Fig.91: Ids vs Vds curves

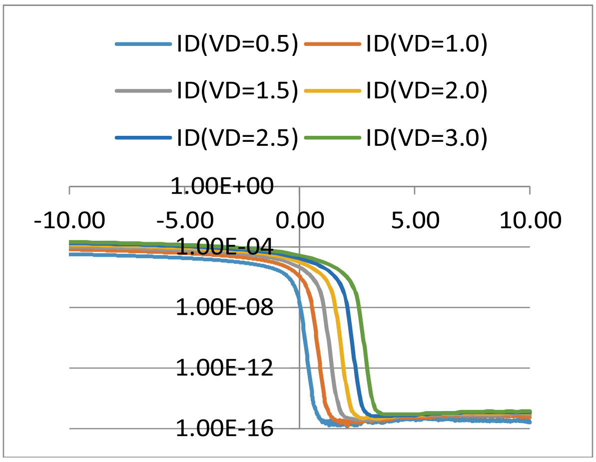


Fig.92: Ids vs Vgs curves

NW thickness 25nm:

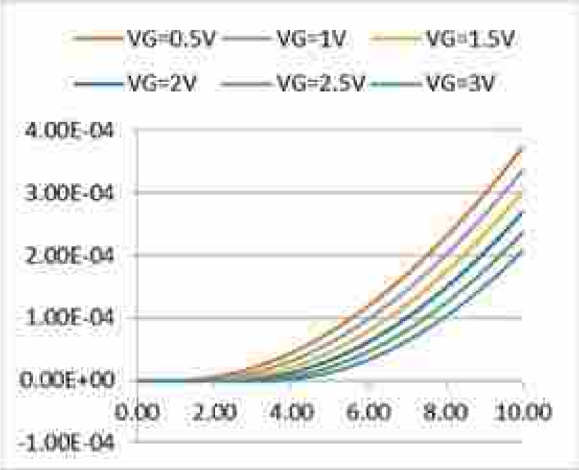


Fig.93: Ids vs Vds curves

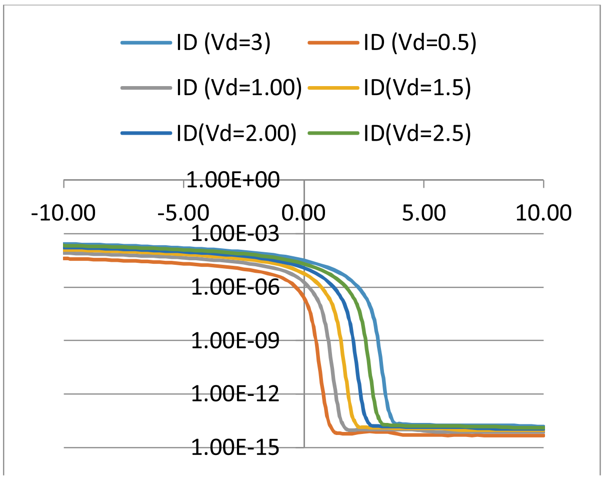


Fig.94: Ids vs Vgs curves

NW thickness 50nm:

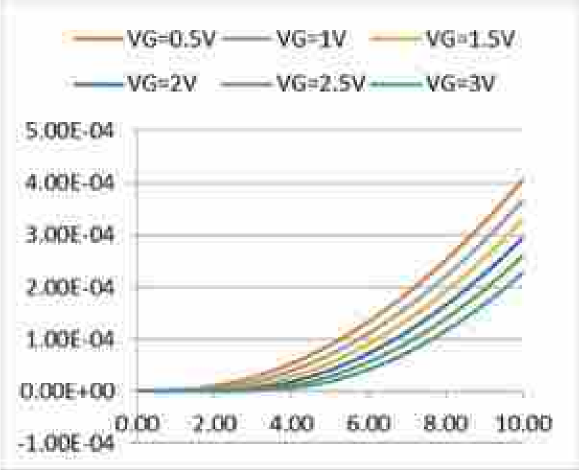


Fig.95: Ids vs Vds curves

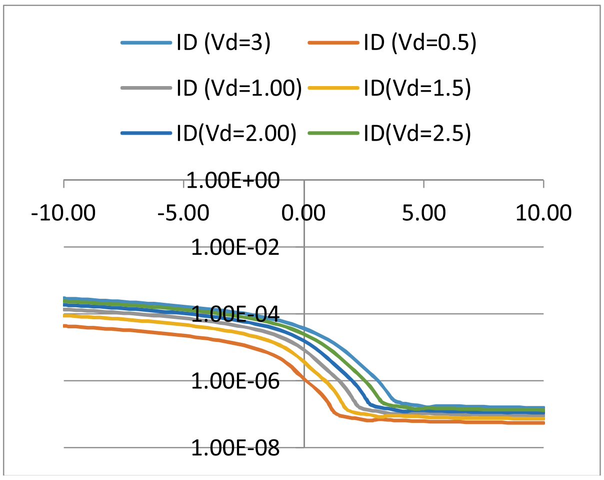


Fig.96: Ids vs Vgs curves

NW thickness 75nm:

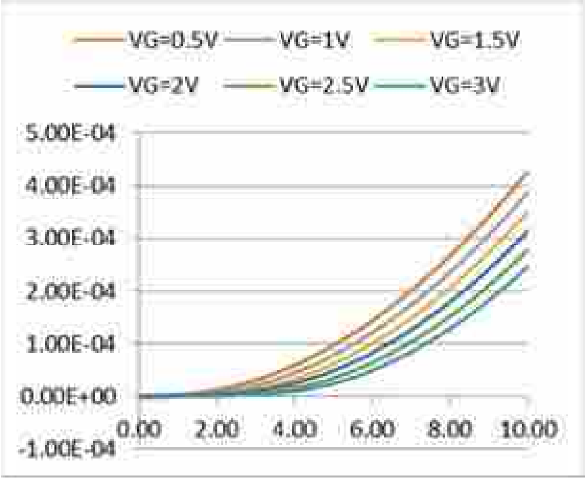


Fig.97: Ids vs Vds curves

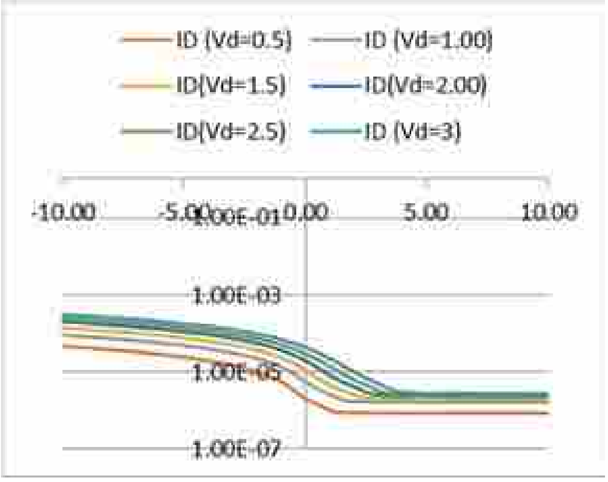


Fig.98: Ids vs Vgs curves

NW thickness 100nm:

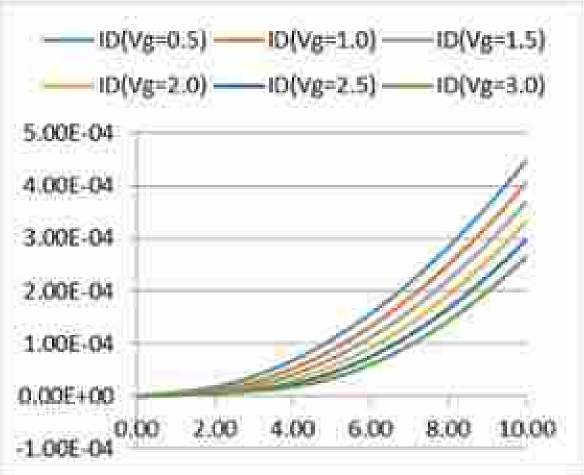


Fig.99: Ids vs Vds curves

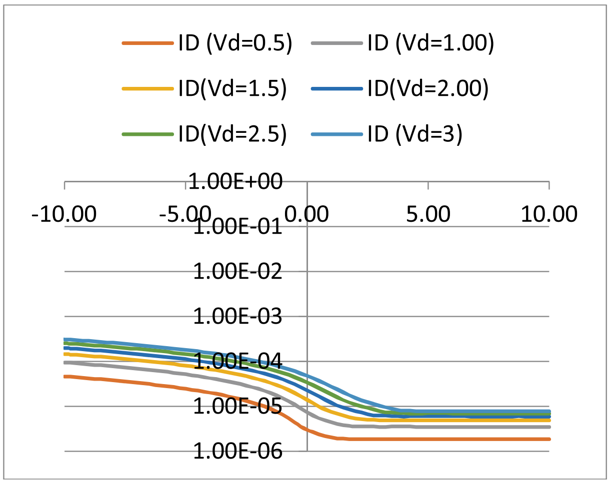


Fig.100: Ids vs Vgs curves

11. 1e18/cm^3

NW thickness 10nm:

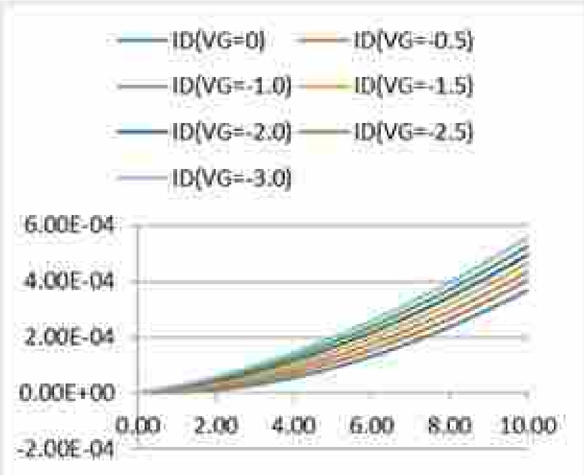


Fig.101: Ids vs Vds curves

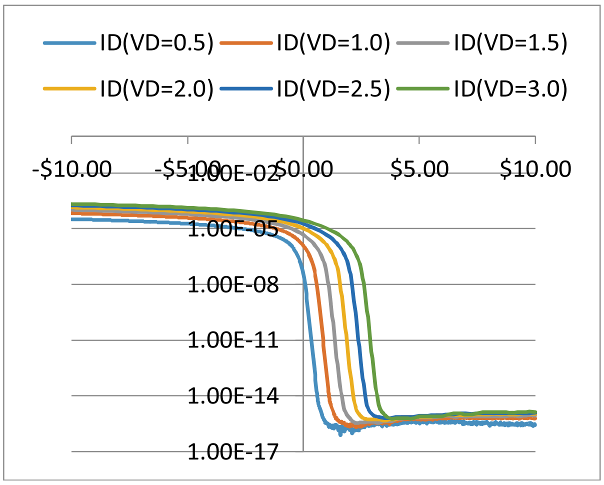


Fig.102: Ids vs Vgs curves

NW thickness 25nm:

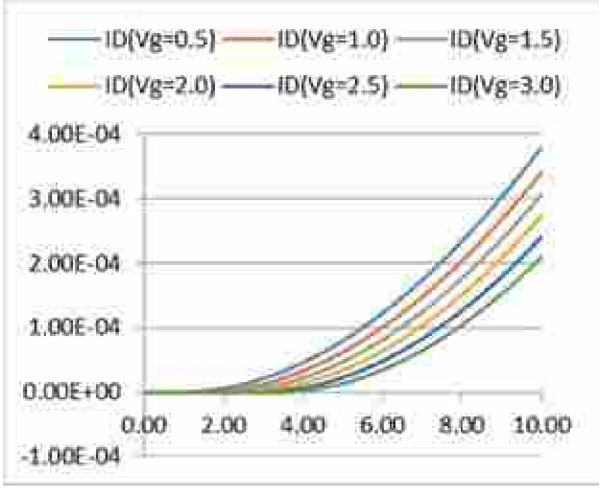


Fig.103: Ids vs Vds curves

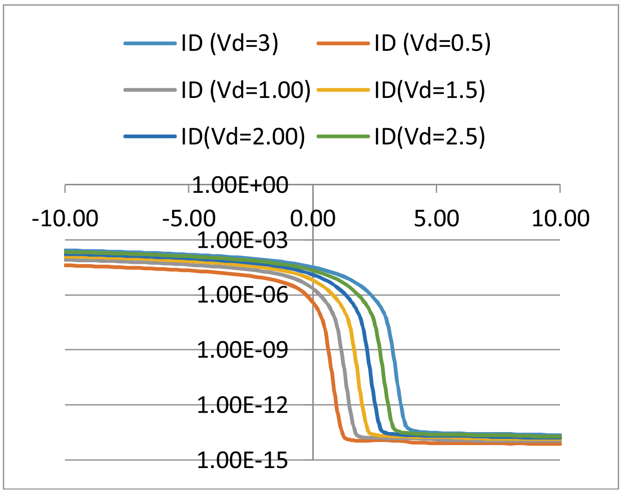


Fig.104: Ids vs Vgs curves

NW thickness 50nm:

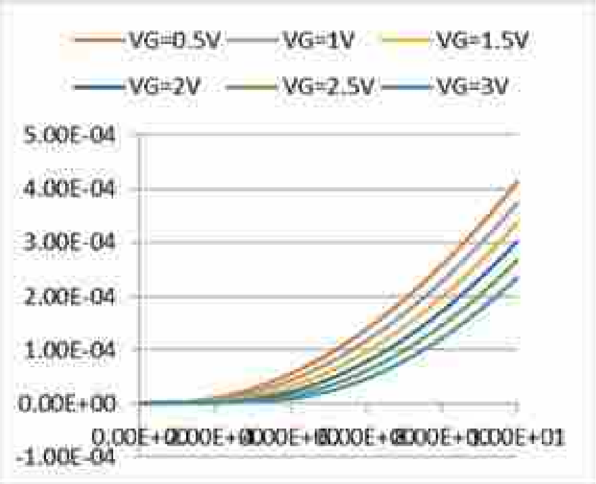


Fig.105: Ids vs Vds curves

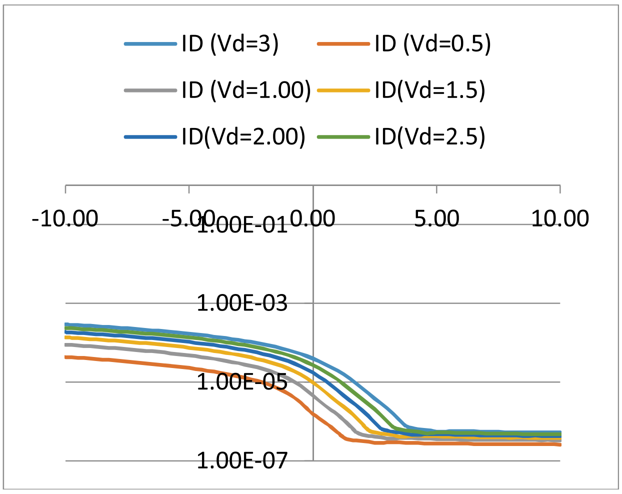


Fig.106: Ids vs Vgs curves

NW thickness 75nm:

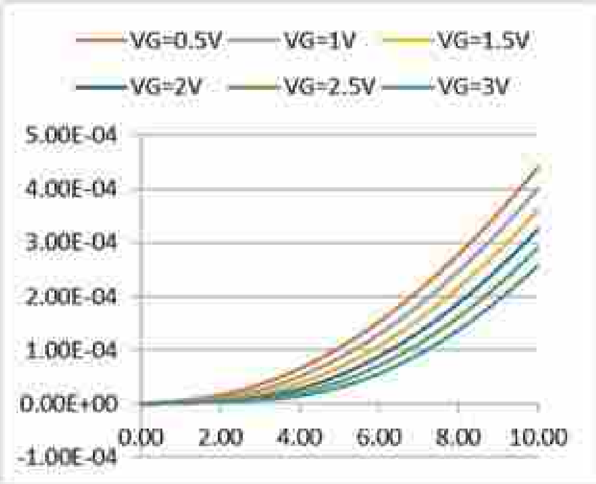


Fig.107: Ids vs Vds curves

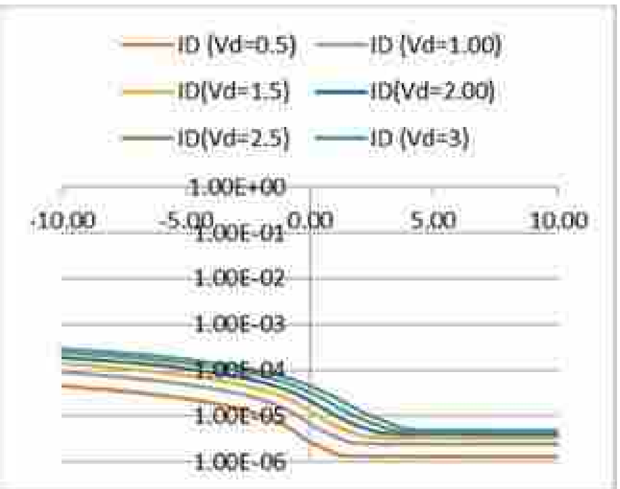


Fig.108: Ids vs Vgs curves

NW thickness 100nm:

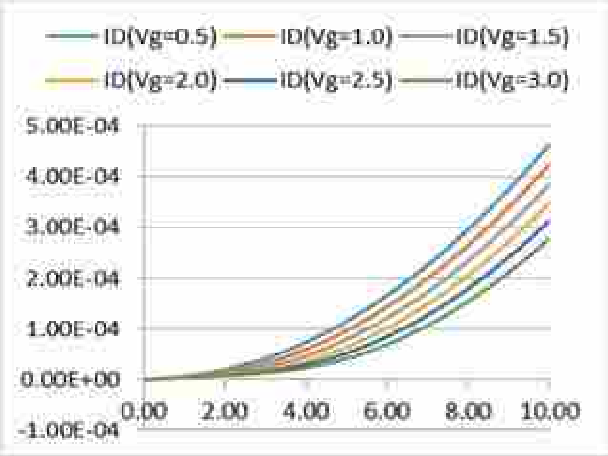


Fig.109: Ids vs Vds curves

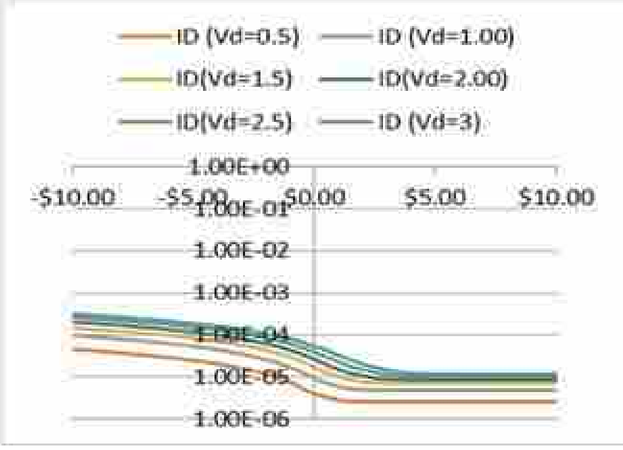


Fig. 110 : Ids vs Vgs curves

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